ADITYA ENGINEERING COLLEGE (A)

VLSI Design-Unit IV

Basic Circuit Design Concepts & Scaling of MOS Circuits

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Course objectives

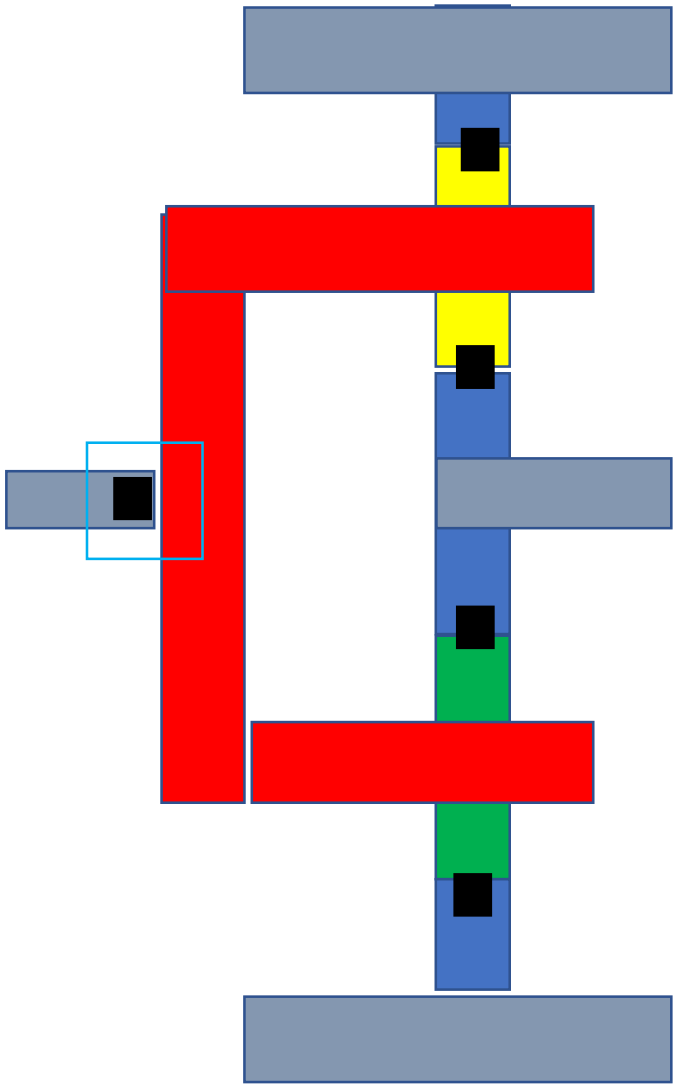
COB 1: To enable the students learn various fabrication steps of IC and MOS, Bi CMOS processes
COB 2: To enable the students learn basic electrical properties of MOS Transistors in analysis of circuits.
COB 3: To make the students to study MOS technology-specific stick and layout rules
COB 4: To make students to familiar with different circuit related parameters
COB 5: To enable the students to highlight the architecture design issues in the context of IC design

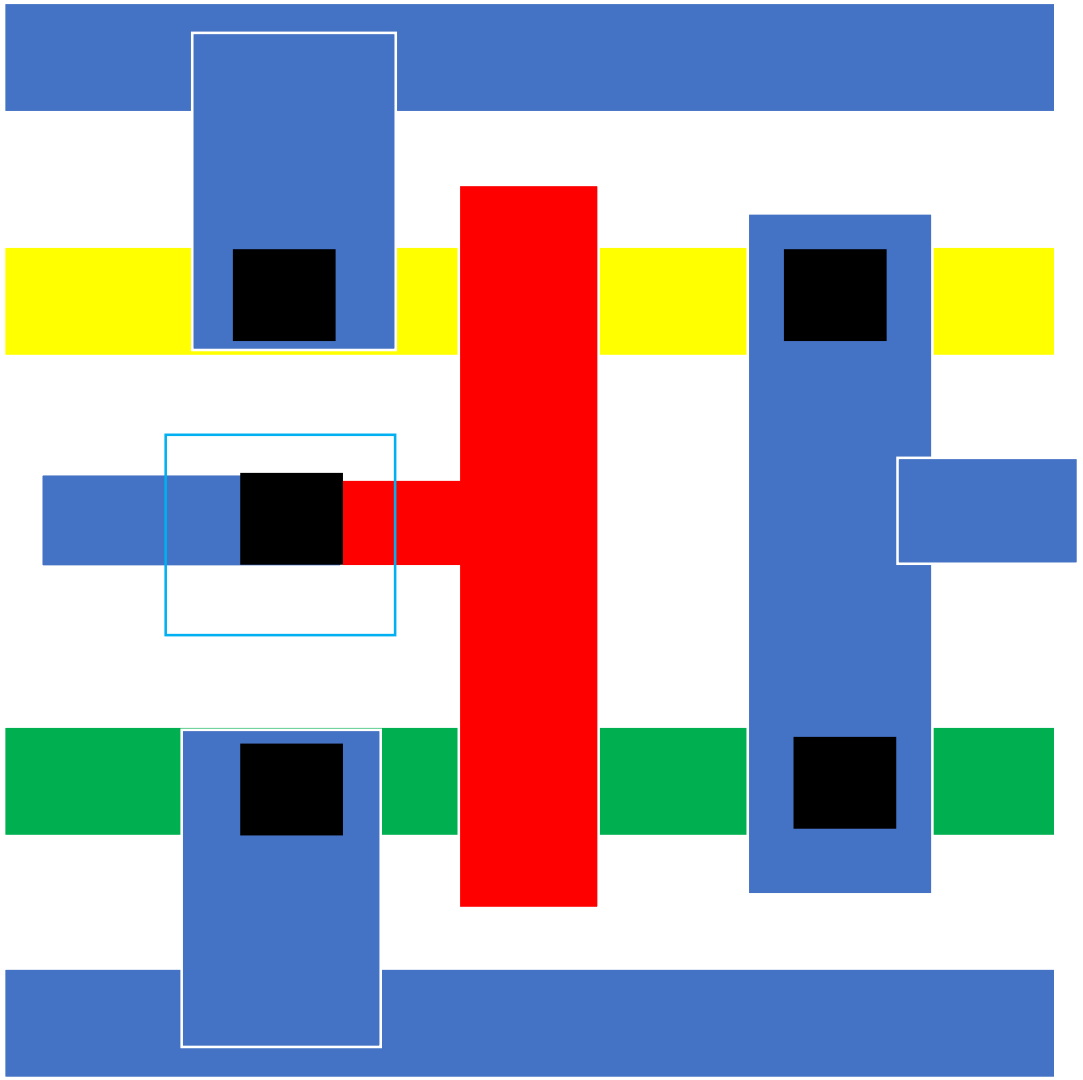
Course outcomes

At the end of the Course, Student will be able to:

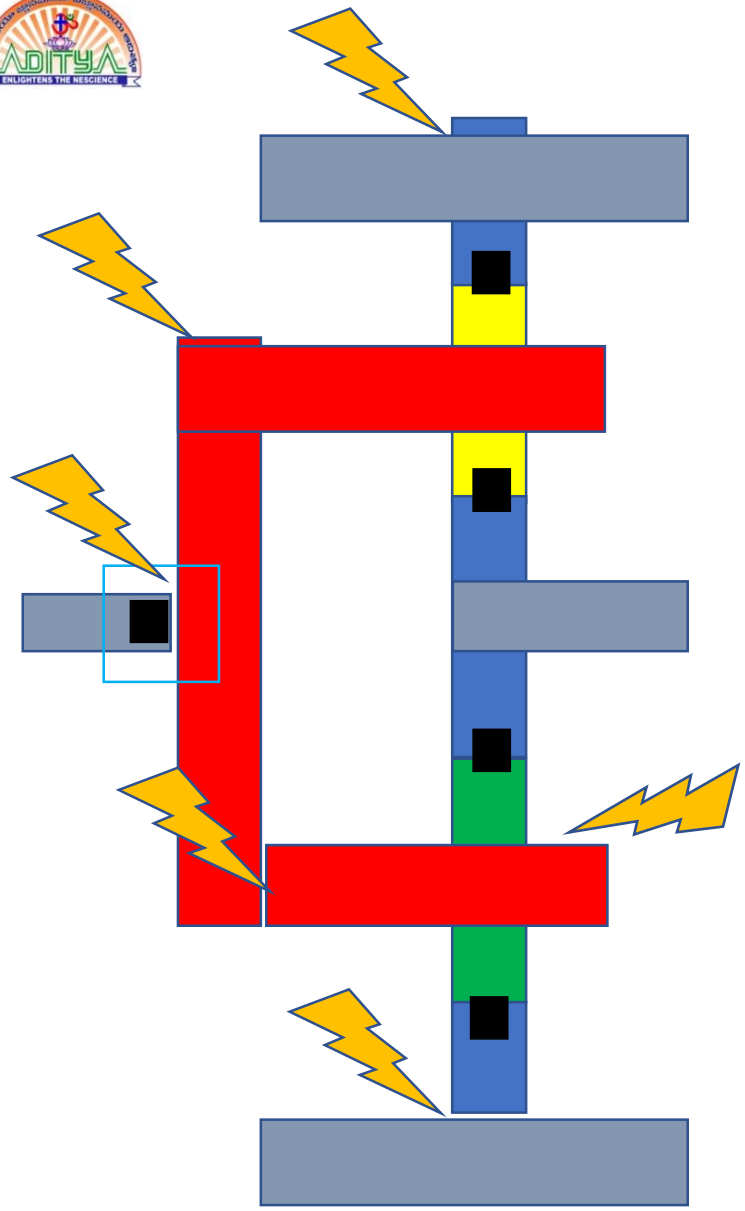
CO1: Outline the fundamental concepts related to MOS and Bi-CMOS Circuits fabrication.
CO2: Analyze the electrical properties of MOS and Bi-CMOS Circuits.
CO3: Make use of design rules for stick and layout diagrams.
CO4: Infer the circuit parameters in modeling the logic/subsystem performance.
CO5: Interpret FPGA and ASIC design approaches for semi custom design

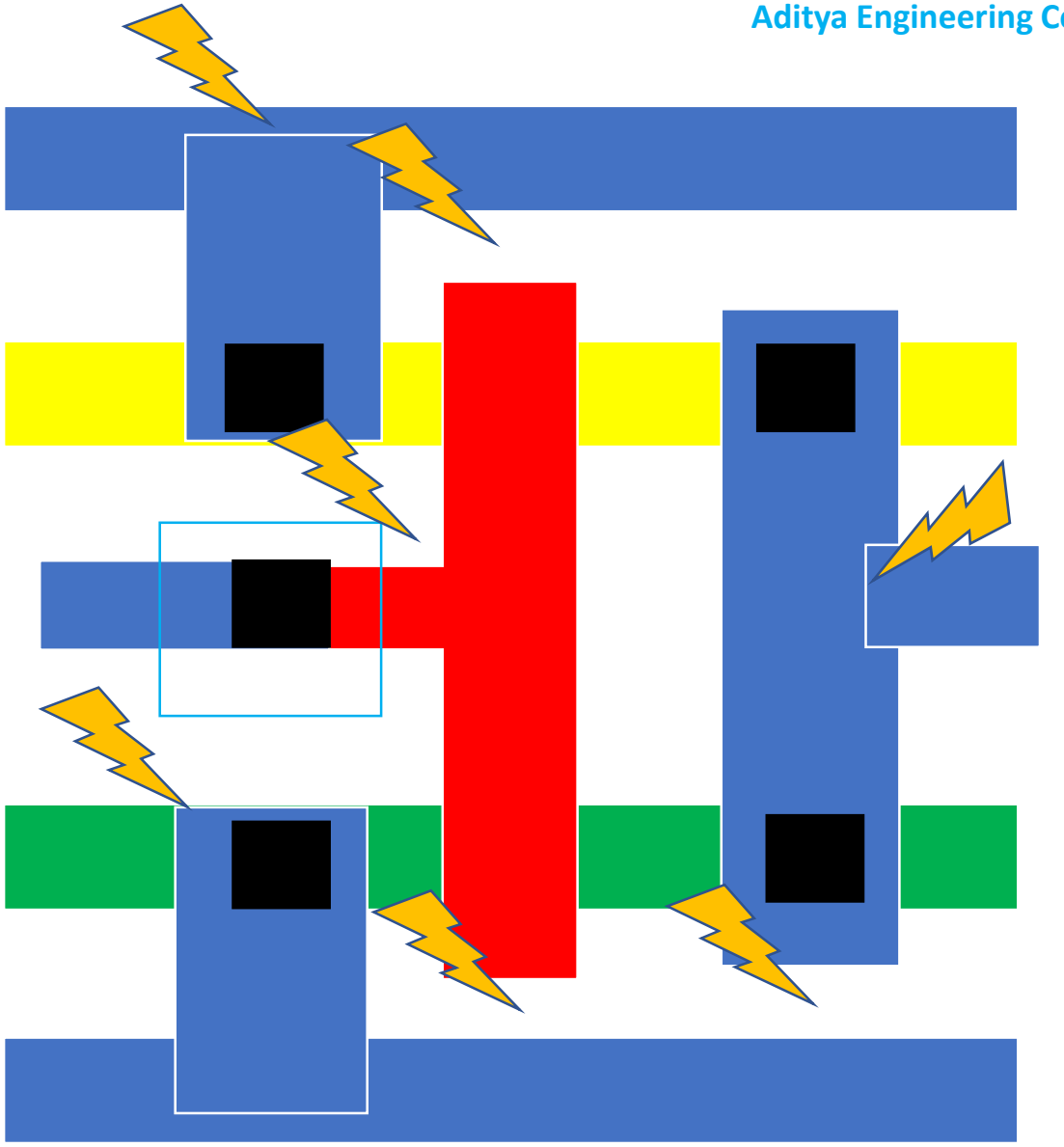
https://personalpages.hs-kempten.de/~vollratj/Microelectronics/2017_04_24_06_Micro_DesignRules.html





Identify the points where there is possibility for DRC violations





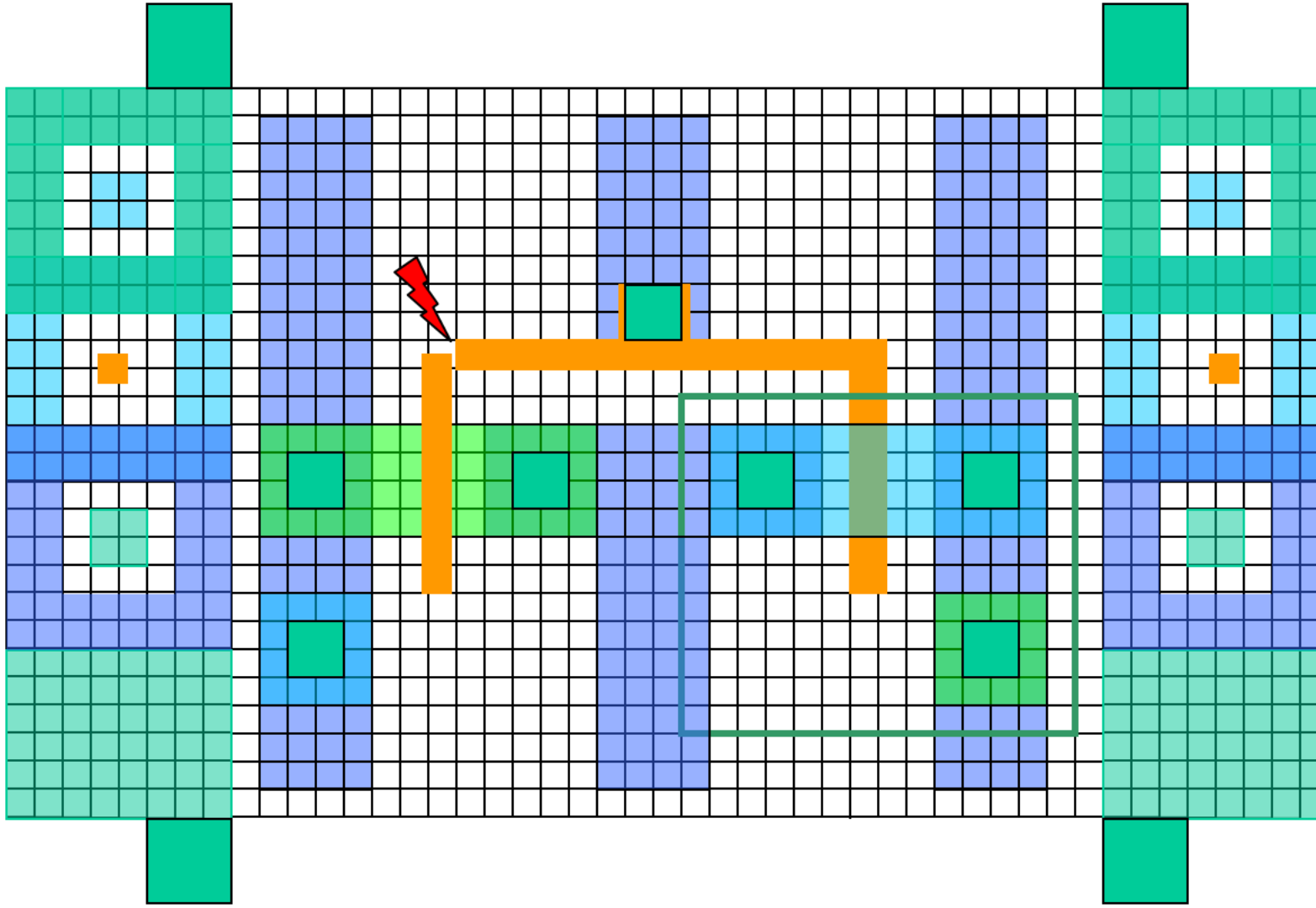
Solution

•Minimum feature size
•Minimum distance or spacing
•Minimum overlap or extension

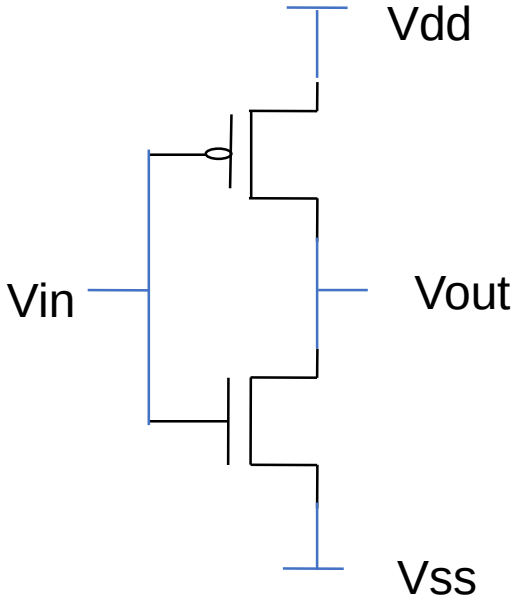
From Circuit to Chip

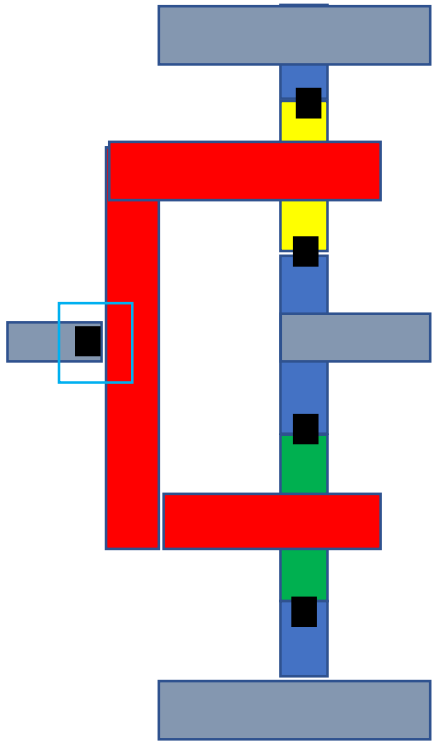
•Circuit design
•Layout with design rules (CAD system)
•Merge with test structures, merge to reticle
•Design rule check with program
•Generation of mask data
•Mask Fabrication: glass and chrome
•Step and repeat:
•Projection of mask onto photo resist on the chip

Over etch, smaller lines causing opens



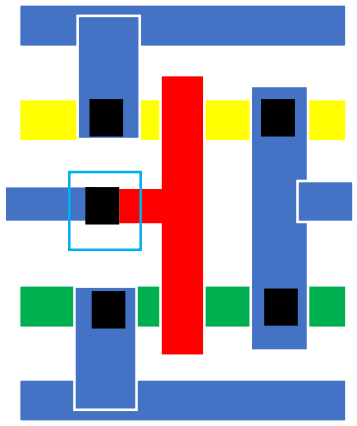
Vout=Vin'

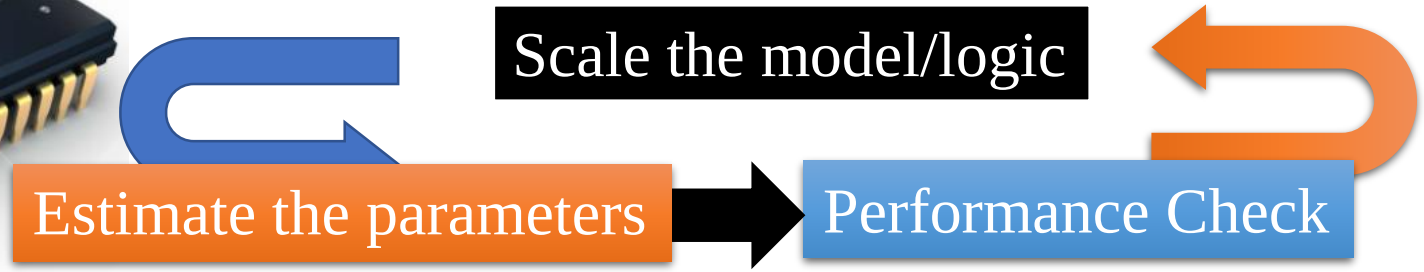




- Define the statement from the problem.
- Draw the truth table
- Write Boolean expression for the outputs.
- Simplify the Boolean expressions
- **Draw the RTL (gates)diagrams**
- Write HDL codes(in different styles)
- Verify the synthesis report
- Draw the schematics(in different types)
- Simulate and check (power & **delay**)
- Draw the layout for the best schematic
- Physical verification(PEX-**parasitic's**)
- **Estimate C, R, Tr, Tf, Delays**

what is known as ckt. design concepts





UNIT-IV

Basic Circuit Design Concepts & Scaling of MOS Circuits

Basic Circuit Concepts:

- Sheet Resistance, and Sheet Resistance concept applied to MOS transistors and Inverters,
- Area Capacitance of Layers, Standard unit of capacitance,
- The Delay Unit, Inverter Delays, Propagation Delays,
- Wiring Capacitances.

Scaling of MOS Circuits:

- Scaling models, Scaling factors for device parameters,

Subsystem Design:

- Architectural issues, switch logic, Gate logic,
- Structured design, clocked sequential circuits,
- System considerations,
- The design process of the arithmetic processor.

Basic Circuit Concepts

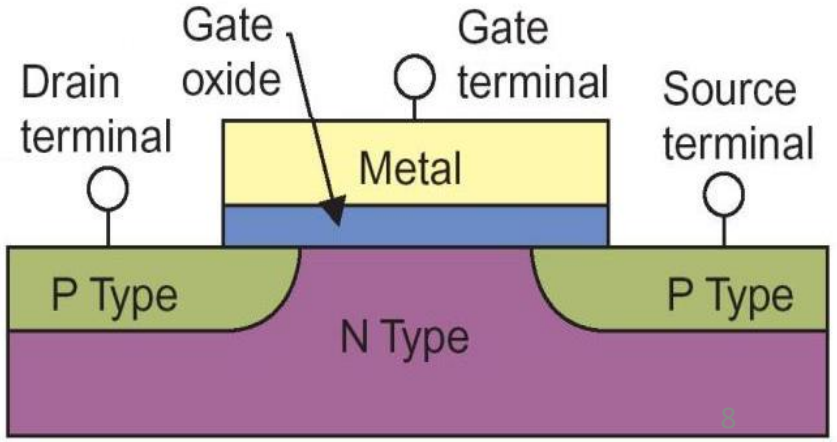
- Introduction:

MOS Transistor is with gate, source and drain forming regions which consists of

S ← ▪ p+ or n+ diffusion
O ← ▪ polysilicon and
M ← ▪ metal layers

Separated by insulating layers

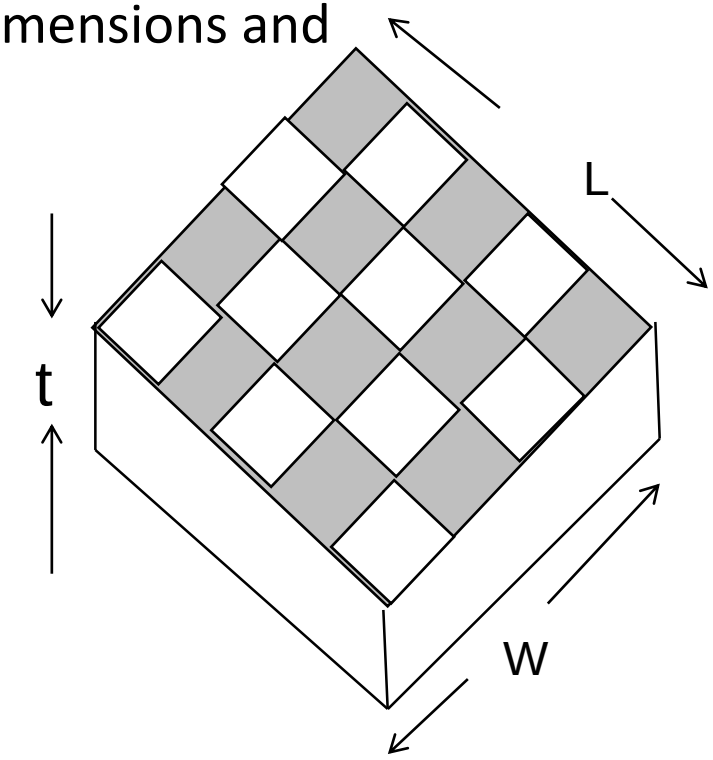
- Each layer has fundamental components like.,
  - Resistance ,Capacitance and Inductance
- Hence, the characterization and performance can be estimated by knowing .,
  - R,C, L, and associated Delays
  - Power & Clock distribution through Tr size
  - Power consumption& Charge Sharing Mechanism
  - Effects of scaling and Reliability



1. Sheet Resistance,

- A uniform slab of semi-conducting material is shown in fig with the dimensions and the resistance of the slab is given by

$$R = \frac{\rho L}{A} = \frac{\rho}{t}\frac{L}{W}$$ Which can be $$R = R_s\left(\frac{L}{W}\right)$$



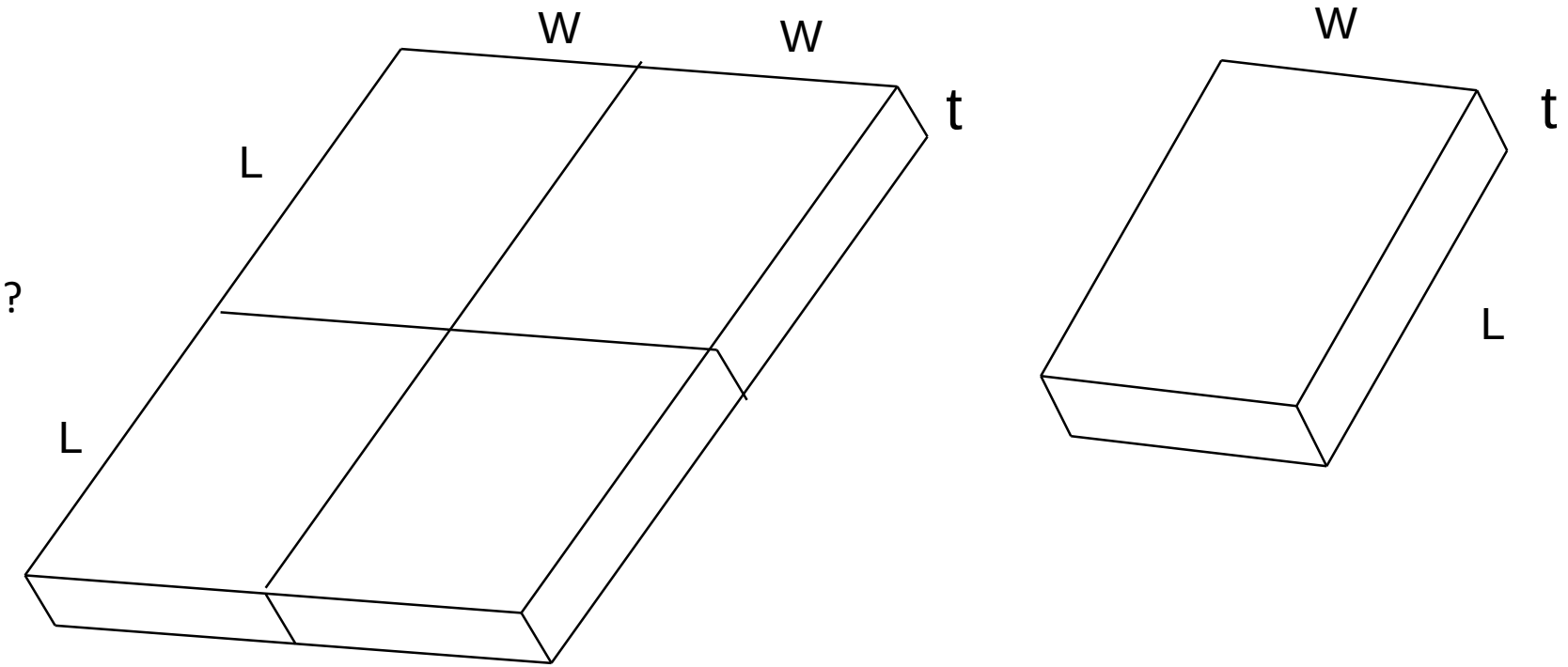
- Where ρ is resistivity of the oxide layer
  - t; is the oxide thickness
  - L; is length oxide slab
  - W; is the width of slab
  - R_s is the sheet resistance in Ω/ □
- Here the sheet resistance Rs depends on only resistivity

  and thickness of the oxide layer but not on length and width of the slab
- On resistance of a slab or MOSFET is given by $R_{on} = Z\ R_s$ with Z as aspect ratio of pull up or pull down device

Sheet Resistance and area dependence,

- The resistances of layers shown in below two figures are equal because of equal thickness and same value of resistivity

resistances of two layers ?



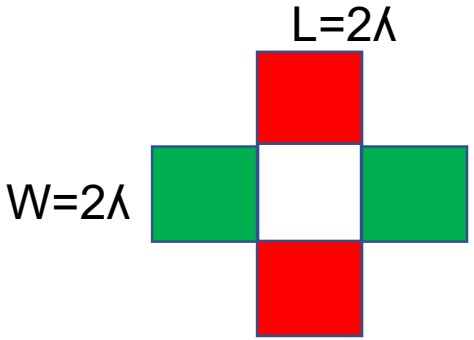
$$R_{\text{large}} = \frac{\rho}{t}\frac{2L}{2W} = \frac{\rho}{t}\frac{L}{W} = R_{small}$$

Rs concept applied to MOS transistors and Inverters

- Consider the two transistor layout structures as shown in below fig. with corresponding dimensions

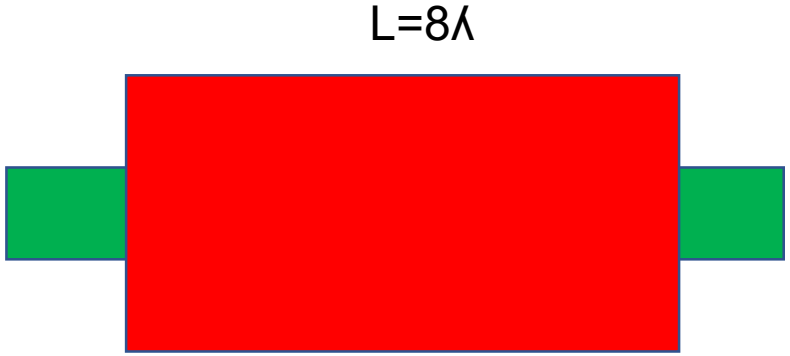
$$R = \frac{\rho L}{A} = \frac{\rho}{t}\frac{L}{W}$$

Fig. a



$$R_a = \frac{\rho}{t}\frac{2\lambda}{2\lambda} = \frac{\rho}{t}(1)$$

Fig. b

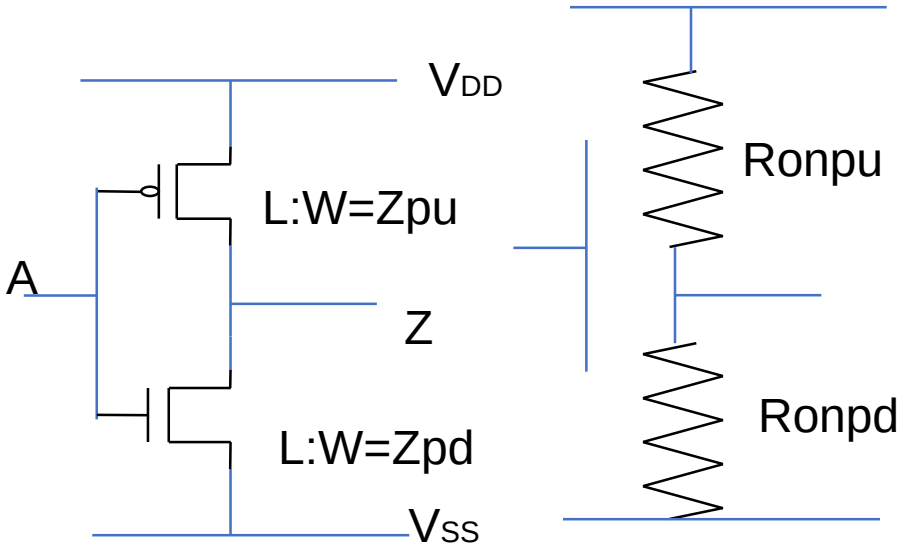


$$R_b = \frac{\rho}{t}\frac{8\lambda}{2\lambda} = \frac{\rho}{t}(4)$$

Therefore, Rb =4 Ra

Problems

Rs concept applied to MOS transistors and Inverters



$$\text{Hence, for an inverter } R_{on} = Z\,R_s$$

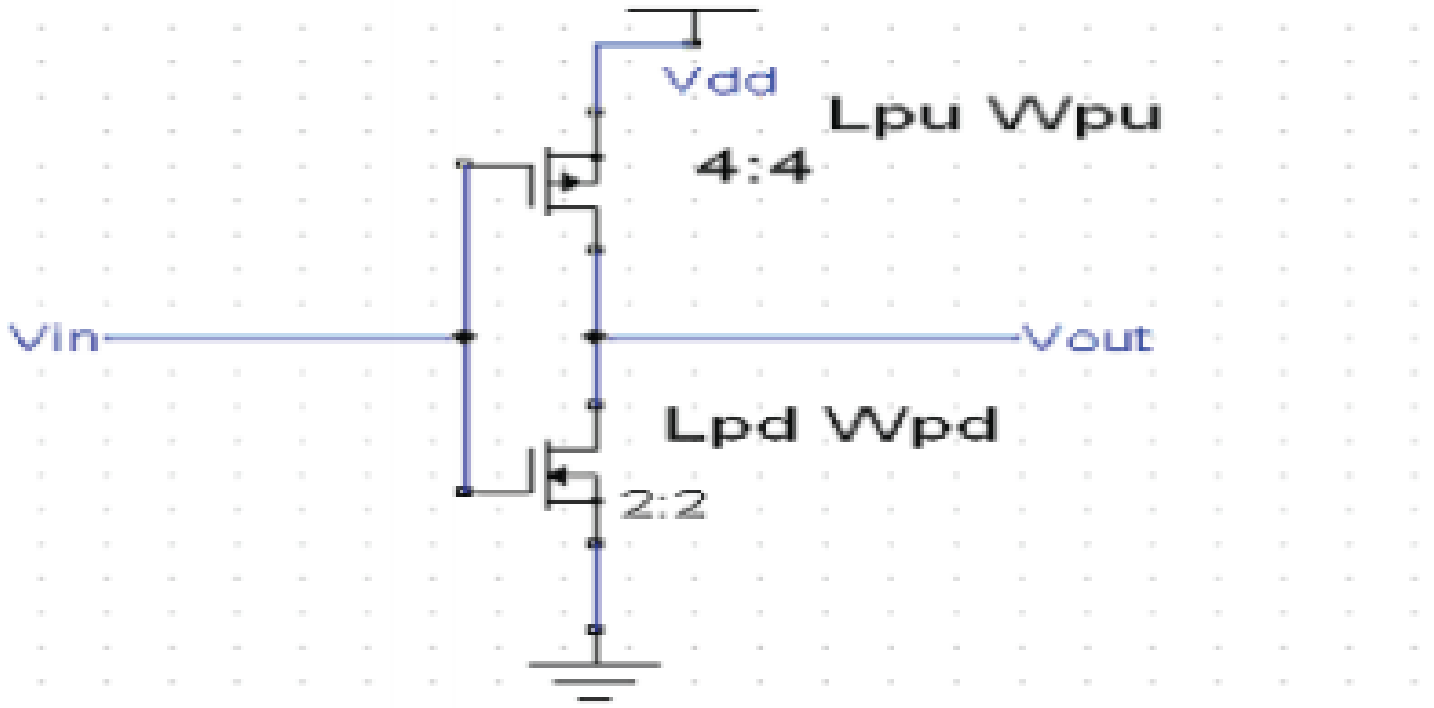
$$R_{ontotal} = R_{onpu} + R_{onpd}$$

$$R_{ontotal} = Z_{pu}R_{sp} + Z_{pd}R_{sn}$$

Problems

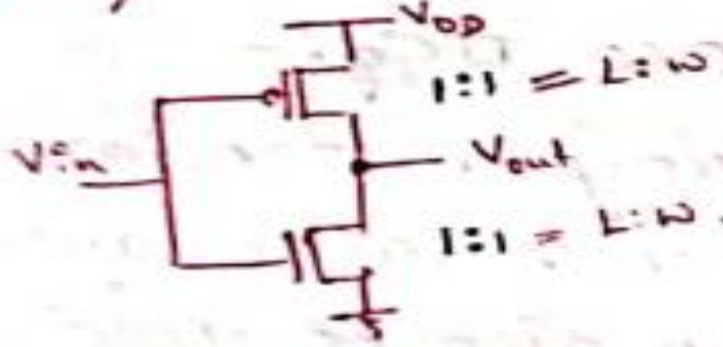
$$R = \frac{\rho L}{A} = \frac{\rho}{t}\frac{L}{W}$$

Calculate on resistance of the circuit shown in the figure 4 from V_{DD} to GND. If n- channel sheet resistance R_{sn}=10^4 Ω per square and P-channel sheet resistance $R_{sp} = 3.5 \times 10^4$ Ω per square. [16]



$$R = \frac{\rho L}{A} = \frac{\rho}{t}\frac{L}{W}$$

Ex 1: Calculate ON resistance of the circuit shown from V_{DD} to Gnd if n-channel sheet resistance $R_{sn} = 10^4\ \Omega/\square$. and p-channel sheet resistance $R_{sp} = 2.5 \times 10^4\ \Omega/\square$.



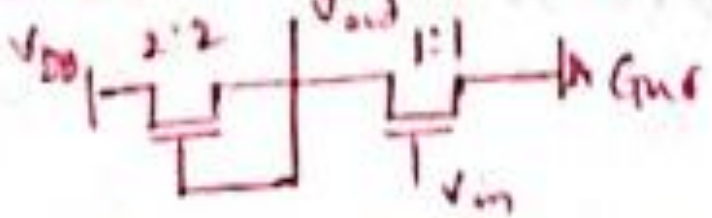
Sol

$$R = \frac{\rho L}{A} = \frac{\rho}{t}\frac{L}{W}$$

Ex 2: Calculate on resistance of the circuit from V_{DD} to Gnd for $R_{sn} = 10^4 \Omega/\square$ and $R_{sp} = 3.5 \times 10^4 \Omega/\square$ with $z_{pu} = \frac{4}{4}$ & $z_{pd} = \frac{2}{2}$.

Sol

Ex 3: Calculate ON resistance from V_{DD} to ground. for given inverter if n channel sheet resistance $R_{sn} = 2 \times 10^4 \Omega/\square$.



Ans = 40KΩ/□.

2. Area Capacitance of Layers

- In a MOS, the conducting layers are separated by dielectric layers, which leads parallel plate capacitive effects.
- For any given layer, the area capacitance can be., $C = \frac{\varepsilon A}{t_{ox}} = \frac{\varepsilon_0 \varepsilon_{ins} A}{t_{ox}}$ farads
- Where t_{ox}=D is thickness of layer(oxide) in cm
- A is area of plate in square cm
- ε_{ins} is relative permittivity of SiO_2 =4.0
- ε_0 is absolute permittivity $8.854X10^{-14}\ F/cm$
- The capacitance of a given area is calculated by taking the product of relative area of the layer and relative area capacitance. i.e.

$$C = \square C_g \ X\left[\frac{Area\,of\ layer\,given}{Area\,of\ \text{standard}\ square}\right] = \square\, C_g\, X\left[\frac{A}{A_{\square}}\right]$$

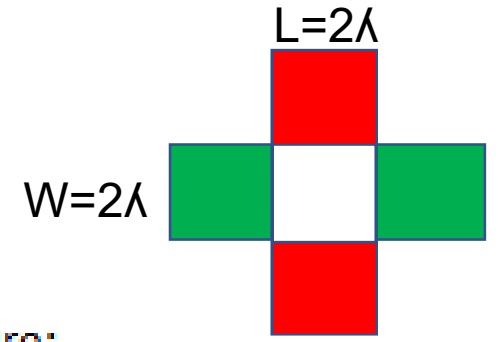
- Where $\square$ Cg is relative capacitance and is technology dependent [given in table]

  A is area of a given layer

  $A_{\square}$ is the area of a standard square in given feature unit(lambda or micron)

Standard unit of Capacitance,

- It is convenient to employ a standard unit of capacitance that can be given a value appropriate to technology but can also be used in calculations without associating it with an absolute value. The standard unit of capacitance is defined as the gate-to-channel capacitance of a MOS transistor having W=L i.e. a standard technology or a feature size as shown in fig, denoted by □Cg
- Here the gate capacitance □ Cg is depending on W & L and may be evaluated for any MOS process



Ex 1: for a 5 um Technology MOS structure;

Area of a standard square is 5umX5um =25 um^2

Capacitance = $4X10^{(-4)}$ pF/um^2

Thus the standard unit of capacitance

□Cg= C_o $A_□$ = $4X10^{(-4)}pF/um^2X25\ um^2$ =0.01pF

Ex 2: for a 2 um Technology MOS structure;

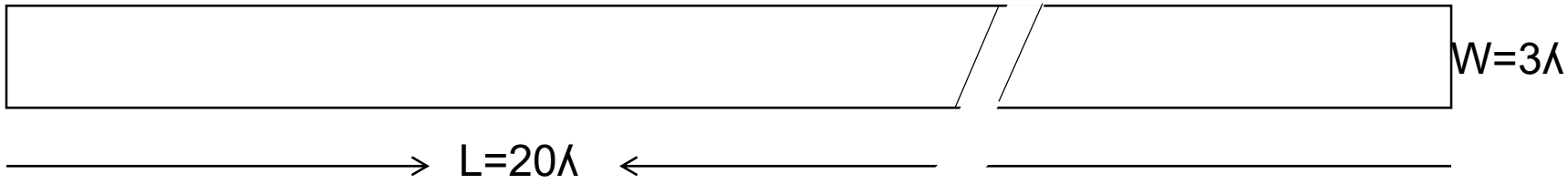
Area of a standard square is 2umX2um =4 um^2

Capacitance = $8X10^{(-4)}$ pF/um^2

Thus the standard unit of capacitance

□Cg= C_o $A_□$ = $8X10^{(-4)}pF/um^2X4\ um^2$ =0.0032 pF

Some area Capacitance calculations



Typical area capacitances in $10^{(-4)}$ pF

Layer name	Technology		
	5um	2um	1.2um
Gate-to-channel	4(1.0)	8(1.0)	16(1.0)
Diffusion (Active)	1(0.25)	1.75(0.22)	3.75(0.23)
Poly-to-substrate	0.4(0.1)	0.6(0.075)	0.6(0.038)
Metal1-to-substrate	0.3(0.075)	0.33(0.04)	0.33(0.02)
Metal2-to-substrate	0.2(0.05)	0.17(0.02)	0.17(0.01)
Metal2-to- Metal1	0.4(0.1)	0.5(0.06)	0.5(0.03)
Metal1-to-Poly	0.3(0.075)	0.3(0.038)	0.3(0.019)

Some area Capacitance calculations

Ex 1: for a 5 um Technology MOS structure;

Area of a standard square is 5umX5um =25 um^2

Capacitance = $4X10^{(-4)}$ pF/um^2

Thus the standard unit of capacitance

☐ $Cg = C_0 A_{\square} = 4X10^{(-4)} pF/um^2 X 25\ um^2 = 0.01pF$

Typical area capacitances in $10^{(-4)}$ pF

Some area Capacitance calculations

C= □Cg(A/ $A_{□}$)

Where ; A is the area of given layer =3λX20λ= 60 $λ^2$

$A_{□}$ is the area of a standard square when L=W

= 2λX2λ= 4$λ^2$

C= □Cg[60 $λ^2$/4$λ^2$]= 15X □ Cg

In general, and is said to be common value of any layer with that dimensions

For a metal, relative capacitance is 0.075□Cg and hence

= 15X 0.075 □ Cg=1.125 □Cg

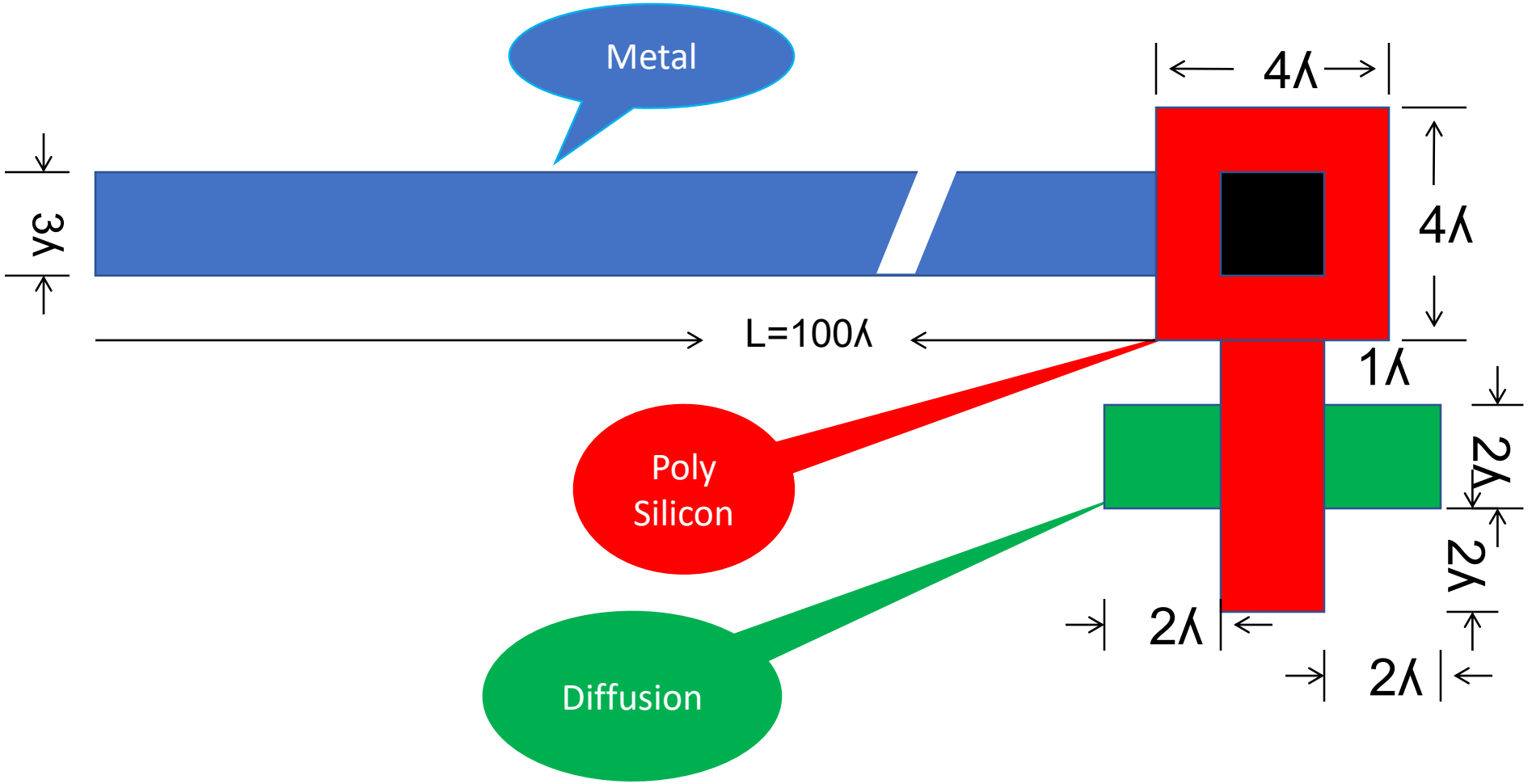
For a polysilicon, relative capacitance is 0.1□Cg and hence

= 15X 0.1 □ Cg=1.5 □Cg

For a diffusion, relative capacitance is 0.25 □Cg and hence

= 15X 0.25 □ Cg=3.75 □Cg

Some area Capacitance calculations



Some area Capacitance calculations: Example

$C = \square C_g(A/A_\square)$

Here, the structure is specified with three different layers. Such as

i) Metal with L=100λ and W=3λ and hence $A_{metal}=3\lambda X100\lambda= 300\ \lambda^2$

ii) Poly with L=4λ and W=4λ, L=2λ and W=2λ,and L=1λ and W=2λ hence $A_{poly}=(4\lambda X4\lambda)+(2\lambda X2\lambda)+(2\lambda X1\lambda)=22\ \lambda^2$

iii) Diffusion with L=2λ and W=2λ, L=2λ and W=2λ and hence $A_{diffusion}=(2\lambda X2\lambda)+(2\lambda X2\lambda)=8\lambda^2$

$A_\square$ is the area of a standard square when $L=W=2\lambda X2\lambda= 4\lambda^2$

As an example, in 2um Technology, the capacitance value is calculated as

For a metal, relative capacitance is 0.075 □Cg and hence

$C_{metal} = \square C_g[300\ \lambda^2/4\lambda^2] = 75X \square C_g = 75X\ 0.075 \square C_g = 5.625 \square C_g$

For a polysilicon, relative capacitance is 0.1 □Cg and hence

$C_{poly} = \square C_g[22\ \lambda^2/4\lambda^2] = 5.5X \square C_g = 5.5X\ 0.1 \square C_g = 0.55 \square C_g$

For a diffusion, relative capacitance is 0.25 □Cg and hence

$C_{diffusion} = \square C_g[8\ \lambda^2/4\lambda^2] = 2X \square C_g = 2X\ 0.25 \square C_g = 0.5 \square C_g$

For a gate, relative capacitance is 1 □Cg and hence

$C_{gate} = 1 \square C_g$

The total capacitance of the given structure is then

$C = C_{metal} + C_{poly} + C_{diffusion} + G_{gate} = 7.675 \square C_g$

3. The Delay Unit

- **The delay unit:** The delay unit τ or a standard delay is defined as "the product of unit area capacitance and a unit n-channel sheet resistance Rs".
- The τ is used as fundamental time unit and all timings in a system can be assessed in relation τ
- by τ = 1.Rs X 1. □Cg
- Rs value and □ Cg value depends on the type of technology that is being used by the designer

For 5um Technology:

1.Rs= 10^4 ohms and 1.□Cg=0.01pF

Ex 1: for a 5 um Technology MOS structure;

Area of a standard square is 5umX5um =25 um^2

Capacitance = $4X10^{(-4)}$ pF/um^2

Thus the standard unit of capacitance

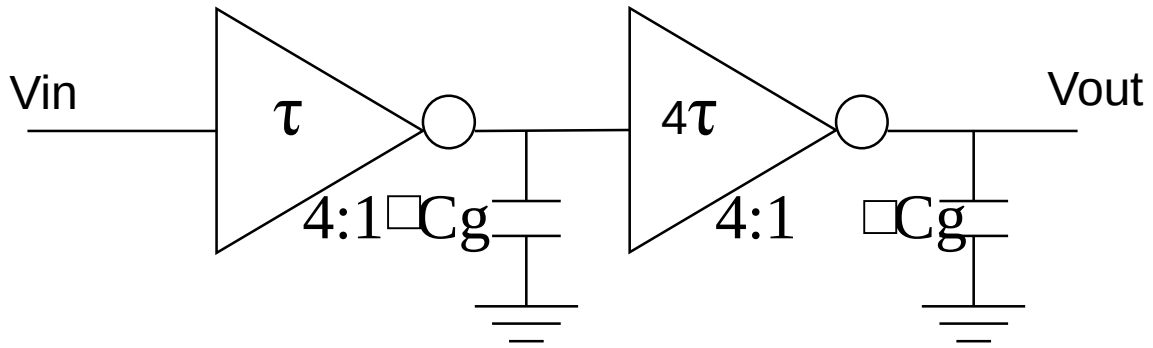
□Cg= C_o A□ = $4X10^{(-4)}pF/um^2X25\ um^2$ =0.01pF

Inverter pair delays

- In a pair of cascaded inverters, the delay over pair will be constant irrespective of logic level transmission at the input to output and is given by

$$T_d = \tau\left[1 + \frac{Z_{pu}}{Z_{pd}}\right]$$

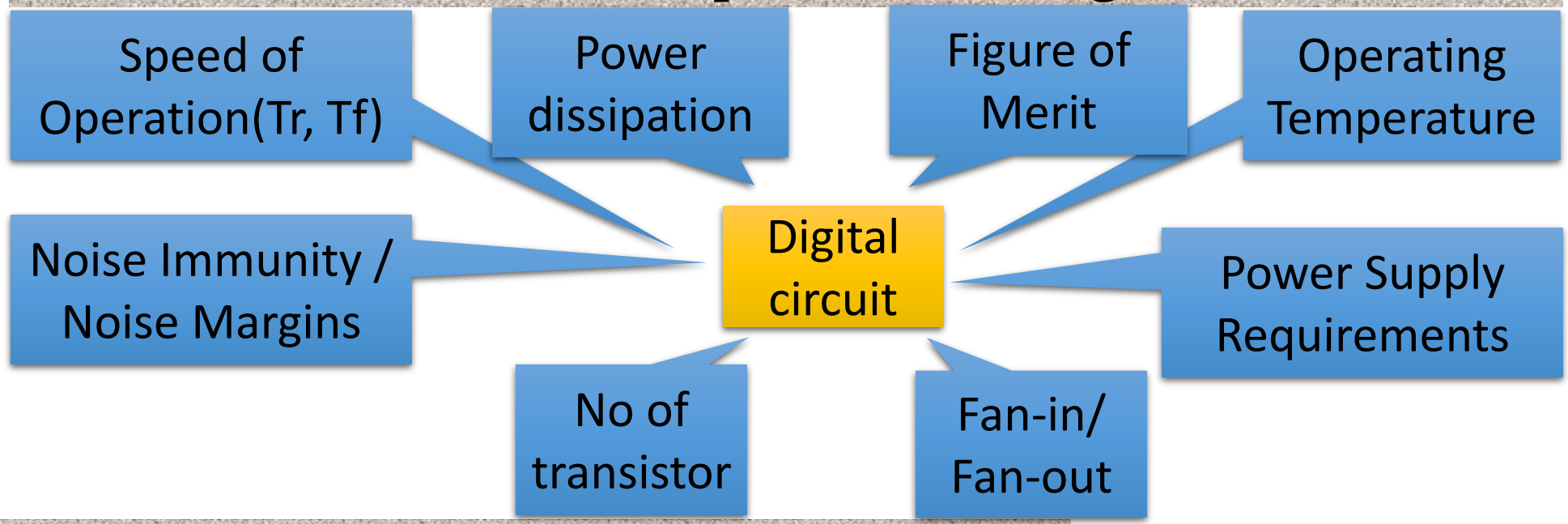
$$T_d = \tau\left[1 + \frac{4}{1}\right]$$



- For a given inverter with (4:1 as Zpu :Zpd), the inverter pair delay is given by
  = 5τ
- Here we need to have Rsp=4 Rsn and Lpu=4Lpd
- In nMOS inverter, the delay is less than the delay in CMOS inverter ,because in CMOS the input is connected to both pMOS and nMOS and hence

C=2 □Cg

The Performance parameters digital circuits



Formal estimation of CMOS inverter delay

The delay associated with the CMOS inverter can be more precisely estimated by splitting the output transition from input into rise time and fall time corresponding to the charging and its discharging of the capacitive load C_L.

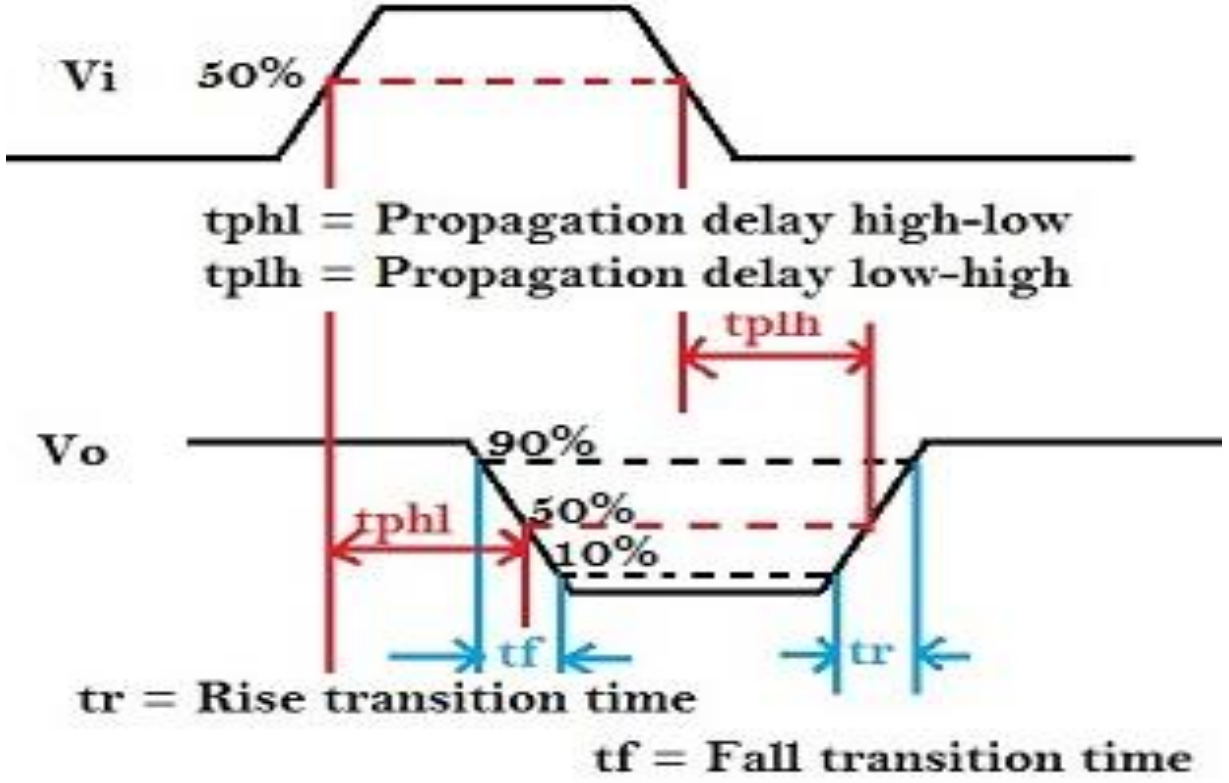
The Switching speed of the CMOS gate is limited by time taken to charge and discharge the load capacitance C_L. Out of the list, Rise time ,Fall time and propagation delay are the primary important.

- Rise time (Tr) is the time, during transition, when output switches from 10% to 90% of the maximum value.
- Fall time (Tf) is the time, during transition, when output switches from 90% to 10% of the maximum value.

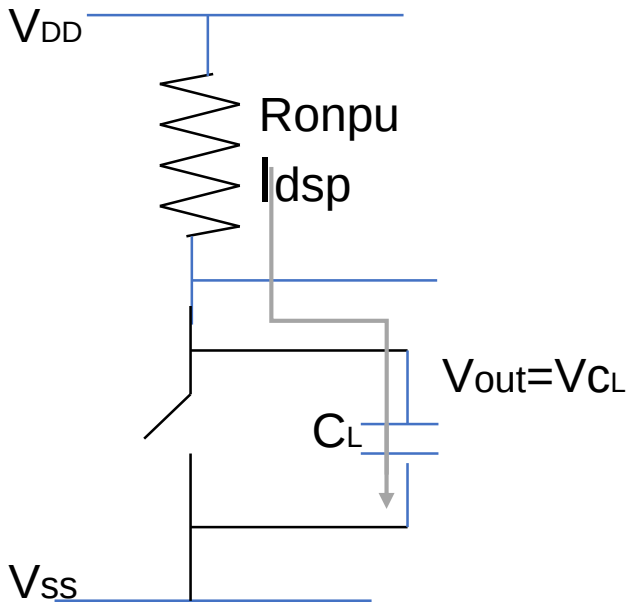
Many designs could also prefer 30% to 70% for rise time and 70% -to-30% for fall time.

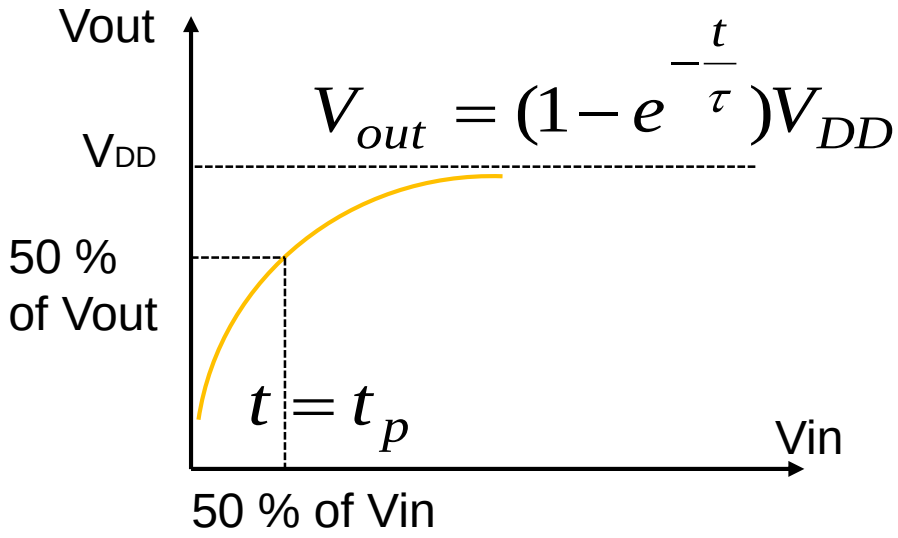
It could vary up to different designs.

The propagation delay of a logic gate is the difference in time (calculated at 50% of input-to-output transition), when output switches, after application of input

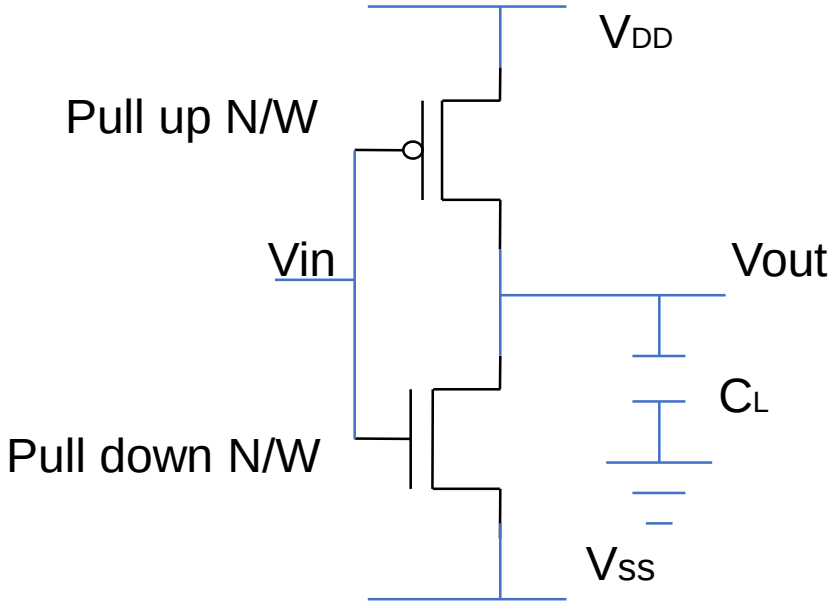


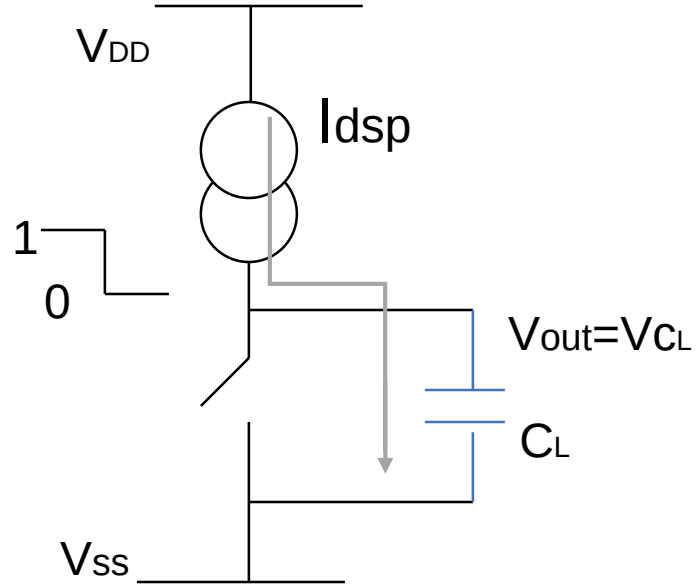
Propagation delay & derivation



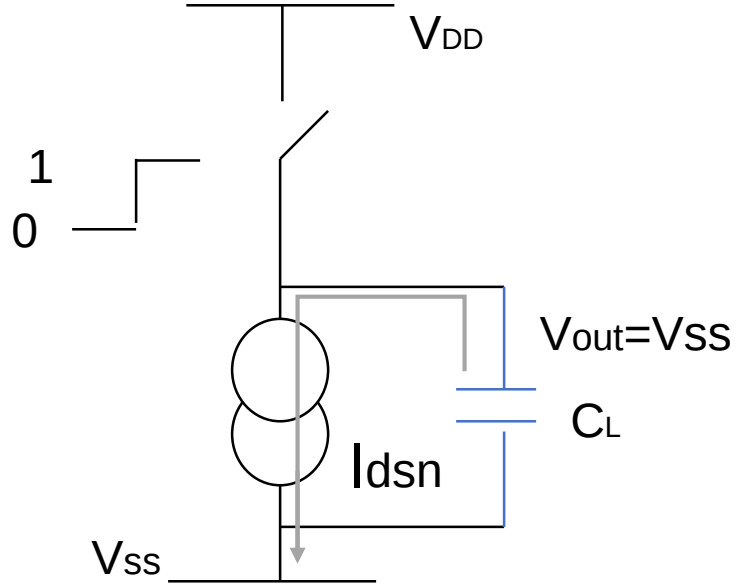


- Our aim is to find ‘t’ at Vdd / 2.
- Vout = $(1-e^{-t/\tau})$ Vdd, where τ = RC = time constant.
- Substituting ‘Vout’ equal to Vdd/2, and ‘t’ equal to ‘tp’ in above eq’n, Vdd/2 = $(1-e^{-tp/\tau})$ Vdd
- Therefore, $t_p = \ln(2)\,\tau = 0.69\tau$ whence, $t_p = 0.69RC$
- Hence, a CMOS inverter can be modeled as an RC network,
- Where R = Average ‘ON’ resistance of transistor &
  C = Output or load Capacitance





Rise time model, CL charges to VDD



Fall time model, CL discharges to VSS

Rise time and fall time estimation

The current that is passing through pMOS transistor when it is in saturation is given by

$$I_{dsp} = \beta_p \left[\frac{(V_{gs} - |V_{tp}|)^2}{2} \right]$$

The output voltage across the load capacitance is given by

$$V_{C_L} = \frac{1}{C_L} \int I_{dsp} dt \quad or V_{C_L} = \frac{1}{C_L} I_{dsp} \int dt \quad \Rightarrow V_{C_L} = \frac{I_{dsp}}{C_L} t$$

$$\Rightarrow t = \frac{V_{C_L}.C_L}{I_{dsp}} = \frac{V_{out}.C_L}{I_{dsp}} \quad \Rightarrow t = \frac{2.V_{out}.C_L}{\beta_p \left(V_{gs} - |V_{tp}|\right)^2}$$

Here
Vgs = VDD and
Vtp = -0.2VDD

T=tr when Vout=Vdd, and hence $\Rightarrow t_r = \frac{2.V_{DD}.C_L}{\beta_p \left(V_{gs} - |V_{tp}|\right)^2} \Rightarrow t_r = \frac{2.V_{DD}.C_L}{\beta_p \left(V_{DD} - |0.2V_{DD}|\right)^2}$

- And hence

$$\Rightarrow t_r = \frac{2.V_{DD}.C_L}{\beta_p\left(1-|0.2|\right)^2.{V_{DD}}^2} \qquad \Rightarrow t_r = \frac{2.C_L}{\beta_p(0.8)^2 V_{DD}}$$

$$\Rightarrow t_r = \frac{2.C_L}{\beta_p 0.64.V_{DD}}$$

$$\therefore t_r \cong \frac{3.C_L}{\beta_p.V_{DD}}$$

As charging and discharging currents are equal

$$\therefore t_f \cong \frac{3.C_L}{\beta_n.V_{DD}}$$

- The fall time is also given by
- The relation between tr and tf is given by $\frac{t_r}{t_f} = \frac{\beta_n}{\beta_p}$ and are not same because of β_n and β_p

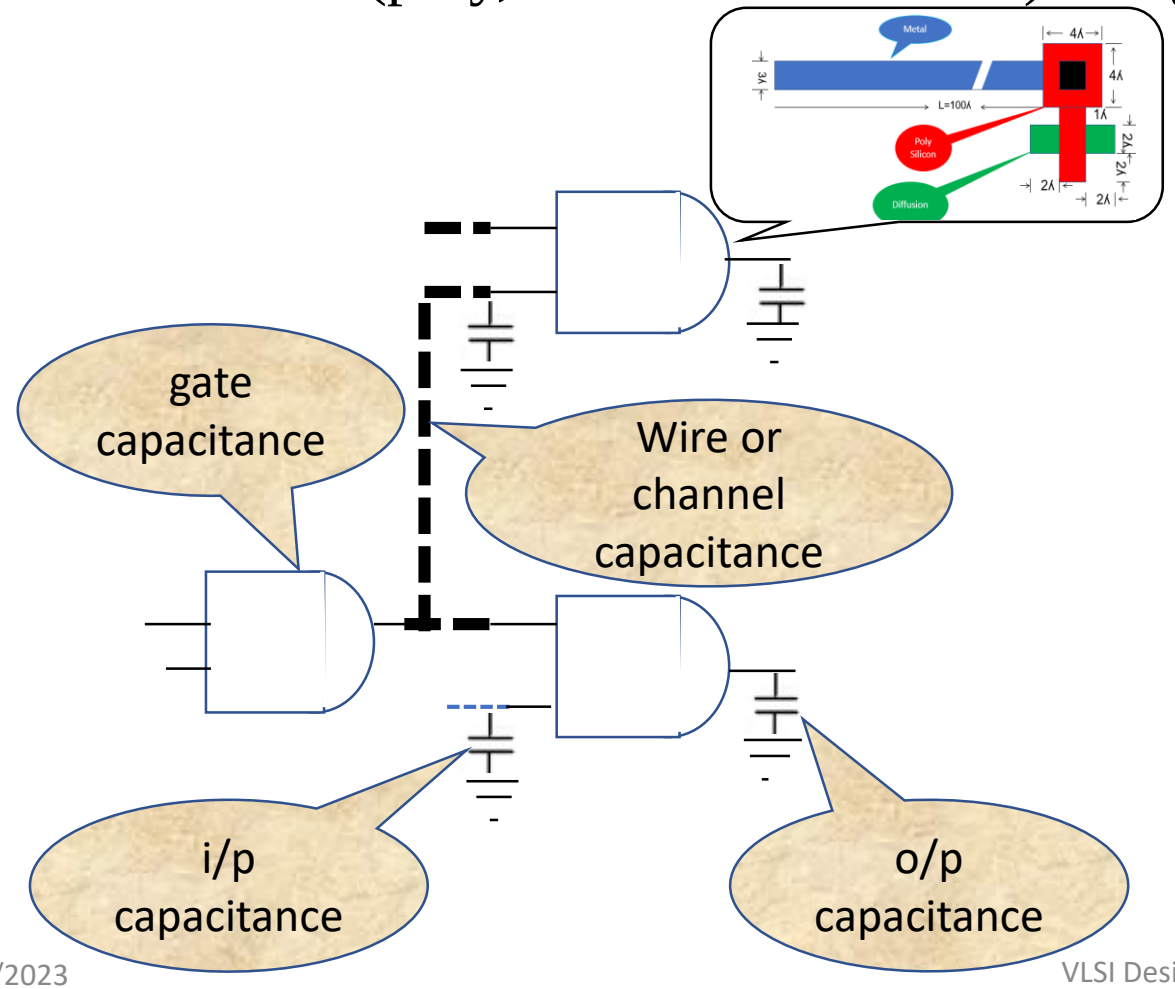
- Here $\beta_n = 2.5\beta_p$ (Since $\mu_n = 2.5\mu_p$) and hence $t_r = 2.5\,t_f$
- The analytical models (shown above) are used for rise time and fall time estimation and will give the optimistic results. However ,
  - The tr and tf are proportional to CL
  - The tr and tf are proportional to 1/VDD and
  - for equal NMOS and PMOS $t_r = 2.5t_f$

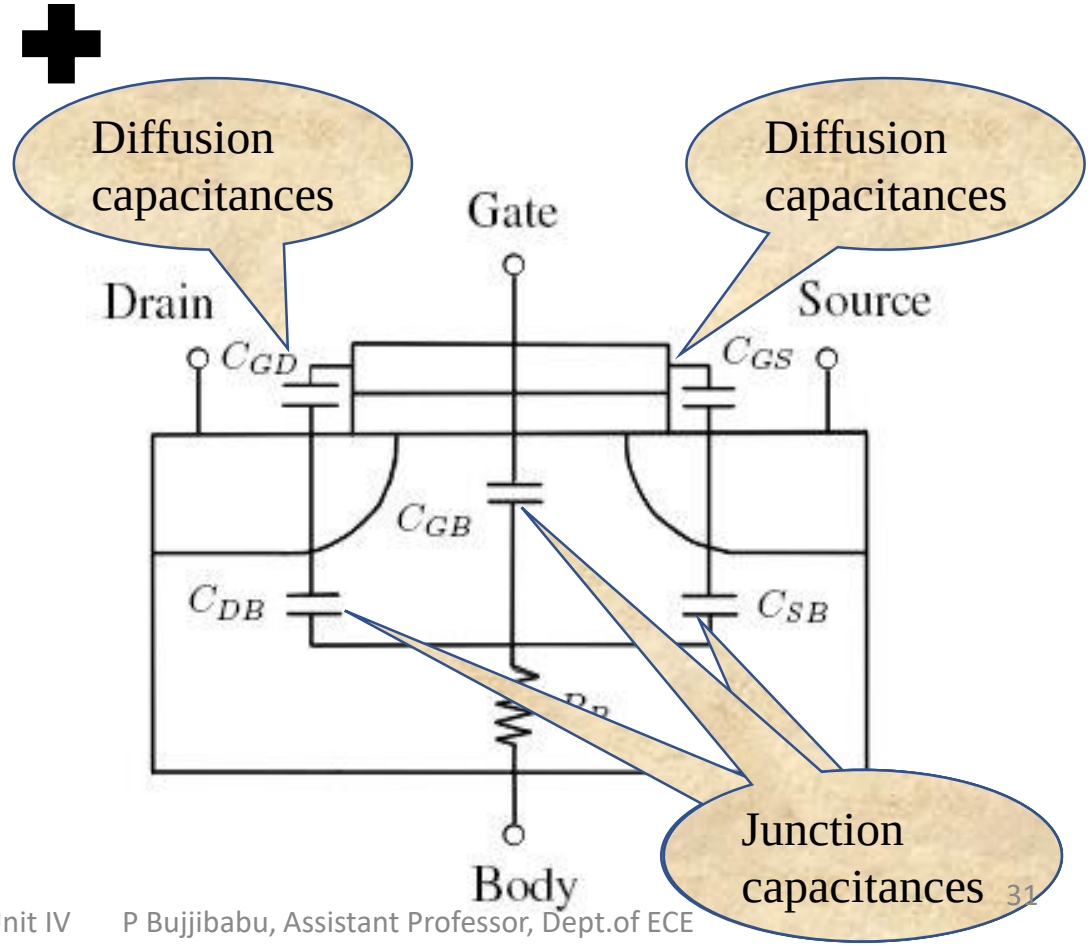
4. Wiring Capacitances

- In a circuit the capacitances are due to the following:

  input capacitance, output capacitance, wire capacitance and gate capacitance(as shown)

In a MOSFET, the associated Capacitive components are shown in below figure, which are due to layer to substrate(poly, metal and diffusion) and gate to channel capacitances respectively.

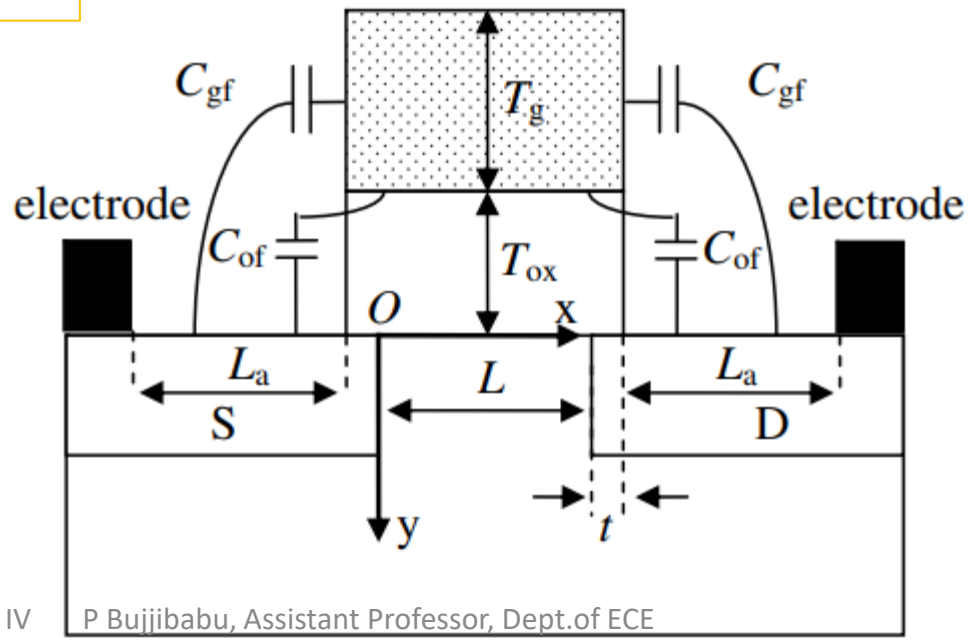




- Out of which wiring capacitance is very significant source of capacitance and is arising due to the following ;
  - Fringing field(Cff) or side wall capacitance.
  - Interlayer capacitance (inside MOS).
  - Peripheral capacitance(outside MOS)
- The fringing field or sidewall capacitance can be modelled as

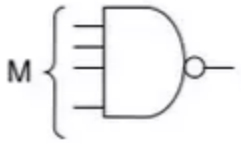
$$C_{gf} = k_1 \frac{2\beta W}{\pi} \cosh^{-1}\left(\frac{T_{ox} + T_g}{T_{ox}}\right)$$

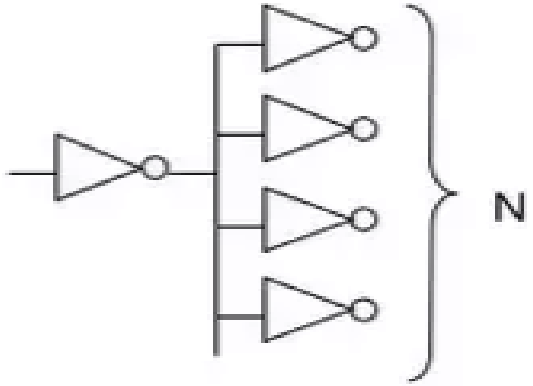
- Where
  - Cgf is gate-to-electrode
  - Cof is gate-to-dielectric
  - β is scaling factor
- Channel or wire capacitance can be calculated in general



Fan in & Fan out characteristics

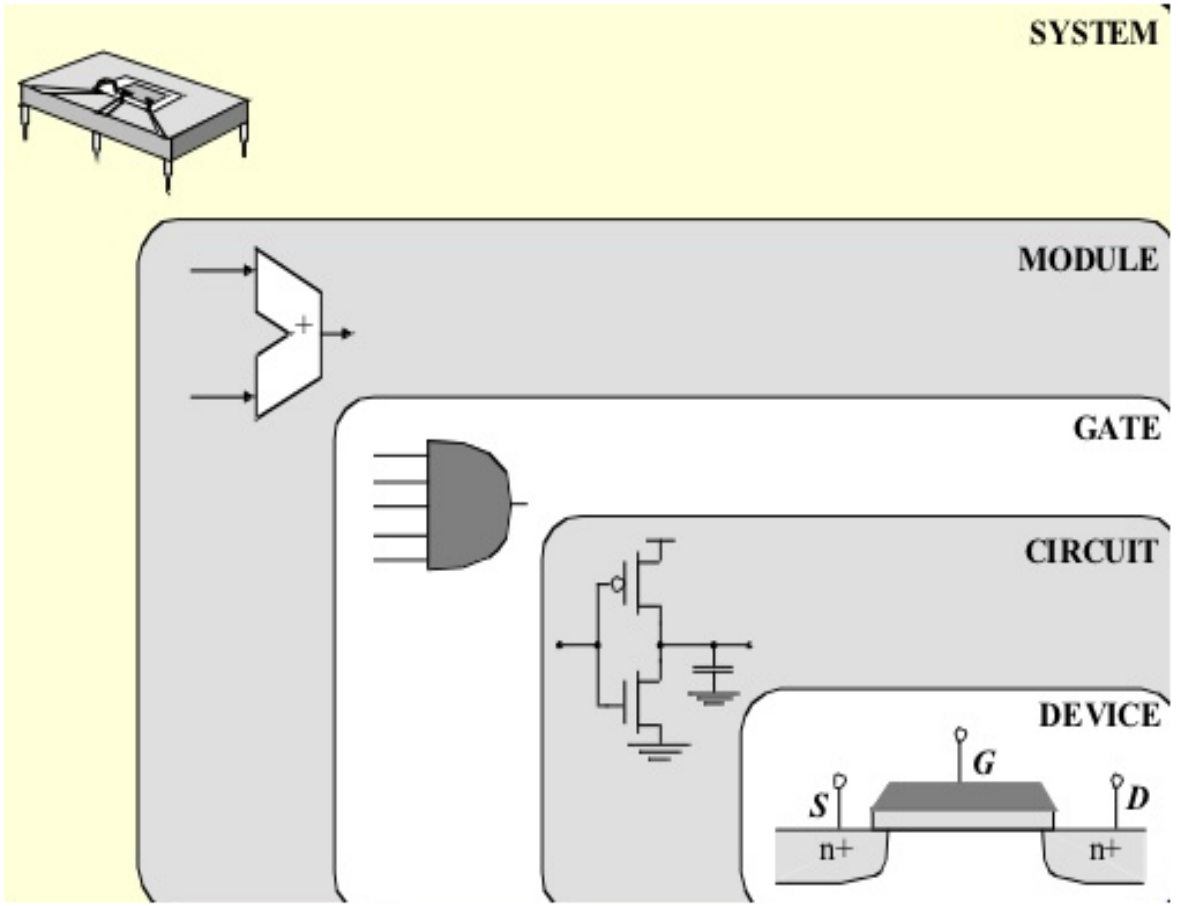
- Fan in is a term used to describe the maximum number of inputs which can be given to a logic gate (logic circuit). For example: A 3-input NAND gate has fan in equal to 3.
- Fan out is a term used to describe the maximum number of gates, an output of another gate (say gate A) can feed i.e how many other gates a single gate can drive.
- Therefore fan out here is mentioned for gate A, that gate which is giving its output as input to other. In the fig below, fan out of NOT gate is mentioned. Not gate can feed less than 4 gates but maximum number of gates it can feed is 4.





Scaling of MOS Circuits

➢ **Scaling models & Scaling factors for device parameters**



Subsystem Design

- Architectural issues,
- Switch logic, Gate logic,
- Examples of structured design,
- Clocked sequential circuits
- System considerations,
- General considerations of subsystem design processes,
- An illustration of design processes

Scaling of MOS Circuits

What is Scaling?

- Proportional adjustment of the dimensions of an electronic device while maintaining the electrical properties of the device, results in a device either *larger* or *smaller* than the un-scaled device.

Why Scaling?...

- Scale the devices and wires down, Make the chips ‘fatter’ – functionality, intelligence,
- memory – and – faster, Make more chips per wafer – increased yield, Make the end user happy

Scaling is characterized in terms of several indicators:

- Minimized feature size or increased number of gates on one chip,
- Reduced power dissipation ,
- Maximum operational frequency ,
- Reduced Production cost
- Fast SOC or NOC design

Scaling of Models and scaling factors:

$$I_{ds} = \frac{\varepsilon_{ins}\varepsilon_0}{D} WL.\mu_n.\frac{1}{L^2}\left(\left[V_{gs} - V_t\right] - \frac{V_{ds}}{2}\right).V_{ds}$$

- The most commonly used models are
  - Constant electric field scaling model
  - Constant voltage scaling model or
  - Hybrid scaling (voltage & dimension) model

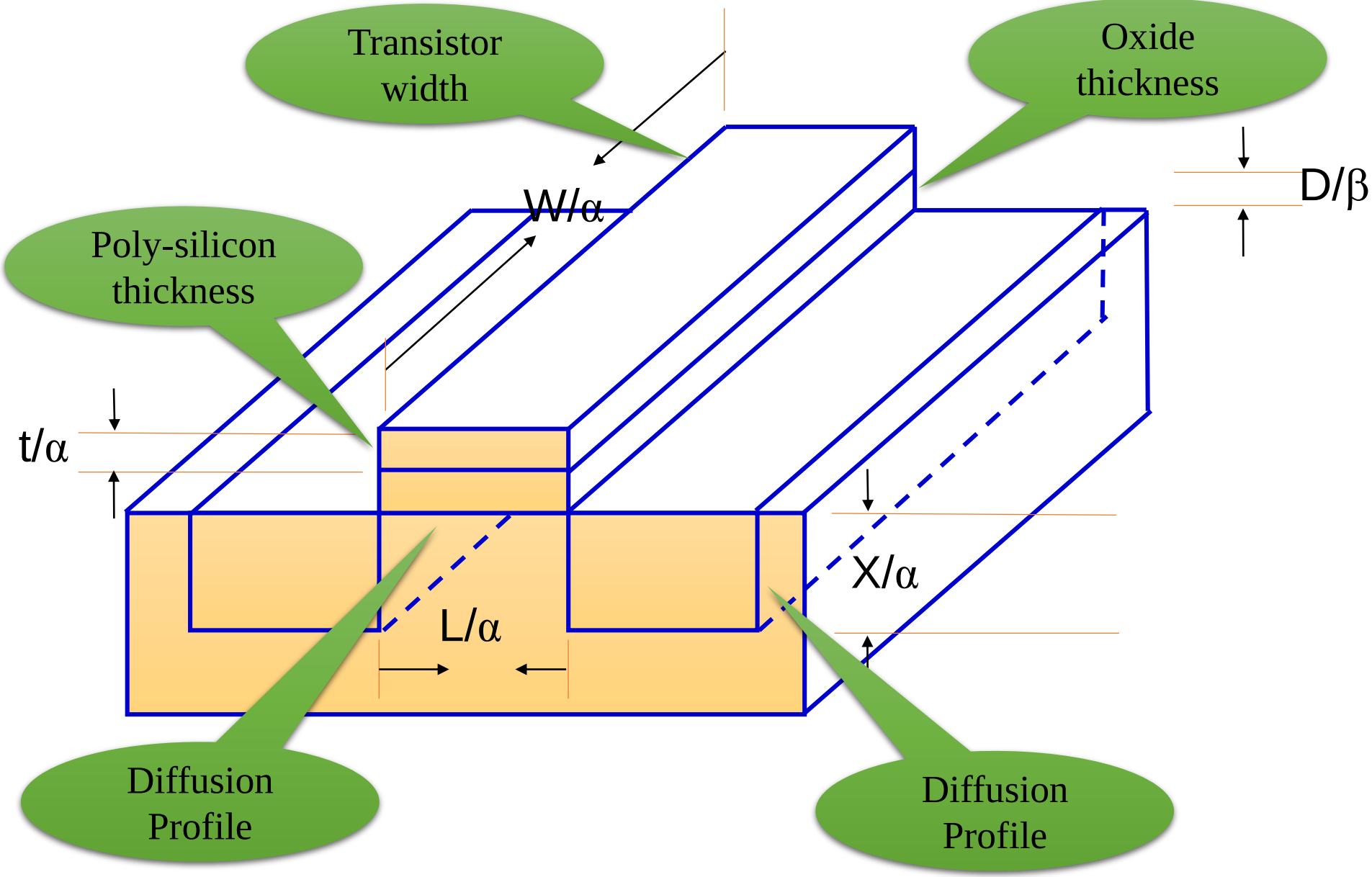
$$I_{ds} = C_g.\mu_n.\frac{1}{L^2}\left(\left[V_{gs} - V_t\right] - \frac{V_{ds}}{2}\right).V_{ds}$$

- In order to accommodate the three models, two scaling factors -1/α and -1/β are used;
- 1/β is a scaling factor used for supply voltages and Oxide thickness(V and D)
- 1/α is a scaling factor used for all other linear dimensions
- For the constant field model and the constant voltage model, β= α=1
- The current/voltage is given by

$$or\ I_{ds} = C_0\mu_n.\frac{W}{L}\left(\left[V_{gs} - V_t\right] - \frac{V_{ds}}{2}\right).V_{ds}$$

Scaling of Models and scaling factors:

- The most commonly used models are
  - Constant electric field scaling model
  - Constant voltage scaling model or
  - Hybrid scaling (voltage & dimension) model
- Constant Voltage (CV)
  - voltage remains constant as feature size is reduced causes electric field in channel to increase
    - decreases performance
  - but, device will fail if electric field gets too large
- Constant Electric Field (CE)
  - scale down voltage with feature size keeps electric field constant
    - maintain good performance
  - but, limit to how low voltage can go



Supply voltages and oxide thickness are scaled by 1/ β

Where as, all other parameters MOSFET are scaled by 1/ α

Scaling factors for device parameters:

It is important that you understand how the following parameters are effected by scaling

- Gate Area
- Gate Capacitance per unit area
- Gate Capacitance
- Charge in Channel
- Channel Resistance
- Transistor Delay
- Maximum Operating Frequency
- Transistor Current
- Switching Energy
- Power Dissipation Per Gate (Static and Dynamic)
- Power Dissipation Per Unit Area
- Power - Speed Product

Scaling factors for device parameters:

- From the MOSFET characteristic equations, we may get the factors as:

➢Gate area (Ag): the gate area of a MOS device is given by Ag=WL

- Both are scaled by $1/\alpha$
- And hence the gate area Ag is scaled by $1/\alpha^2$

➢Gate capacitance per unit area (Co or Cox):

- The gate capacitance of a MOS device is given by $Co=Cox=\varepsilon_{ox}/D$
- D is scaled by $1/\beta$ and hence capacitance is scaled by $1/1/\beta = \beta$

➢Gate capacitance (Cg):

- The gate capacitance or total capacitance Cg is given by Cg=CoWL
-
-

Co scaled by β

W scaled by $1/\alpha$

L scaled by $1/\alpha$

Hence Cg is scaled by β/α^2

➢Parasitic capacitance (Cx):

- The parasitic capacitance of a MOS device is given by

$$Cx=(\varepsilon_x Ax)/t$$

- Ax is scaled by 1/ α and t is scaled by 1/α
- Hence Cx is scaled by 1/α^2

➢Carrier density in channel(Qon):

- The carrier density in channel or charge in the channel is given by

$$Qon = CoVgs$$

- Co scaled by β
- Vgs scaled by 1/β

Hence the Qon is scaled by 1

➢The channel resistance (Ron):

- The channel resistance Ron is given by $R_{on} = \frac{L}{W}\frac{1}{Q_{on}\mu}$
- L,W scaled by 1/α
  Qon scaled by 1
  And hence Ron is scaled by 1

➢Gate delay (Td):

- The gate delay is given by Td= RonCg
- Cg is scaled by β/α^2
  Ron scaled by 1
  And hence Td is scaled by β/α^2

➢Maximum operating frequency(fo=1/Td):

- The operating frequency is scaled by α^2/β

➢Saturation current(Idss):

$$\Rightarrow I_{ds} = C_0\mu_n.\frac{W}{L}\left(\left[V_{gs}-V_t\right]-\frac{V_{ds}}{2}\right).V_{ds}$$

$$\Rightarrow I_{ds} = \frac{C_0\mu_n}{2}\frac{W}{L}\left(V_{gs}-V_t\right)^2 \qquad \Rightarrow I_{ds} = \frac{C_0\mu_n}{2}\frac{W}{L}\left(V_{ds}\right)^2$$

- Hence the I_{ds} s scaled by $\beta \cdot 1/\alpha \cdot 1/1/\alpha \cdot 1/\beta^2 = 1/\beta$

For Co For W For L For Vds

- Current density (J): current density J is given by Idss/A

- Idss scaled by $1/\beta$
- A is scaled by $1/\alpha^2$

And hence J is scaled by $\frac{1/\beta}{1/\alpha^2} = \frac{\alpha^2}{\beta}$

- Advantages and disadvantages with MOSFET scaling:

✓*** short channel effects(DIBL & hot electrons)
✓*** complex process technology
✓*** dominant parasitic effects

Observations on Device scaling

- Gate capacitance per micron is nearly independent of process
- But ON resistance * micron improves with process
- Gates get faster with scaling (good)
- Dynamic power goes down with scaling (good)
- Current density goes up with scaling (bad)
- Velocity saturation makes lateral scaling unsustainable

Limitations of scaling:

- Limits of miniaturization
- Limits of interconnect and contact resistance
- Limits due to sub-threshold currents:

With technology scaling, threshold voltage has to be scaled along with supply voltage, in order to maintain performance

Reduction in Vth increases the sub-threshold leakage current significantly

Sub-threshold leakage is the current that flows between the source and drain of a MOSFET when the transistor is in the weak-inversion region.

Sub-threshold leakage power will increase at a very rapid rate due to its strong dependence on the Vth

- Substrate doping
- Limits on logic levels and supply Voltage due to noise
- Limits due to current density

Subsystem Design

- Architectural issues,
- Switch logic & Gate logic,
- Examples of structured design,
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- System considerations,
- General considerations of subsystem design processes,
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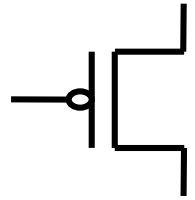
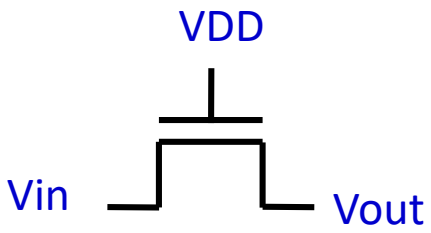
Architectural issues:
concepts applied in larger system design requirements

- Define the requirements (properly & carefully).
- Partition the overall architecture into appropriate subsystem.
- Consider communication paths carefully in order to develop sensible interrelationships between subsystem.
- Draw a floor plan of how the system is to map onto the silicon (and alternate between 2,3 and 4 as necessary).
- Aim for regular structures so that design is largely a matter of replication.
- Draw suitable (stick or symbolic) diagrams of the leaf_cells of the subsystems.
- Convert each cell to layout.

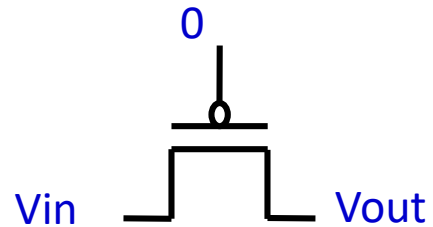
Switch logic & Gate logic: PT logic Examples



nMOS



pMOS



Vout=Vin-Vt

If Vin=0V then Vout = 0 – Vtn
= - Vtn
< = 0V

Strong 0

If Vin=0V then Vout = 0 – (-Vtp)
= + Vtp
> 0V

Weak 0

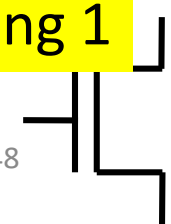
If Vin=5V then Vout = 5V – Vtn
< 5V

Weak 1

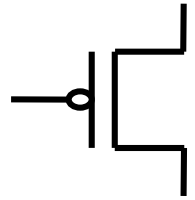
If Vin=5V then Vout = 5V- (-Vtp)
= 5V+Vtp
>=5V

Strong 1

- nMOS passes a good low (0) but not a good high (1)
- pMOS passes a good high (1) but not a good low (0)

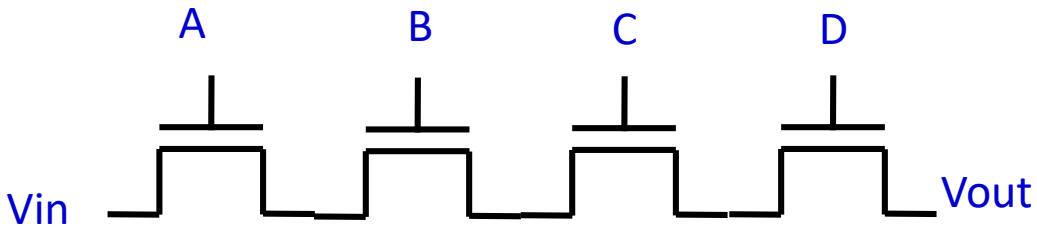


Switch logic & Gate logic: PT logic Examples

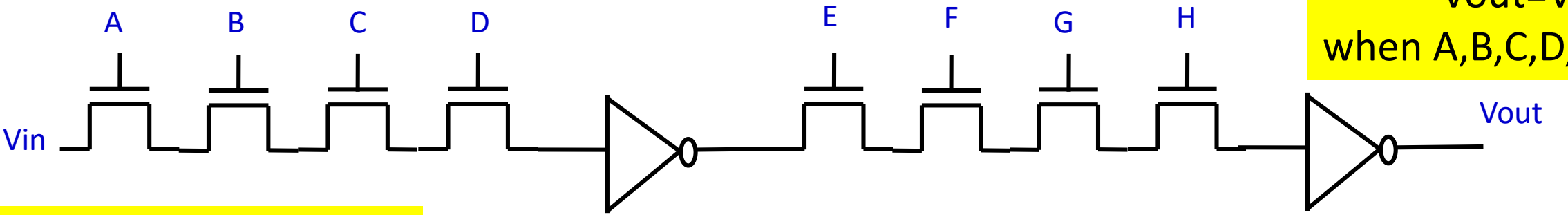


Vout=Vin; when A=B=C=D=1

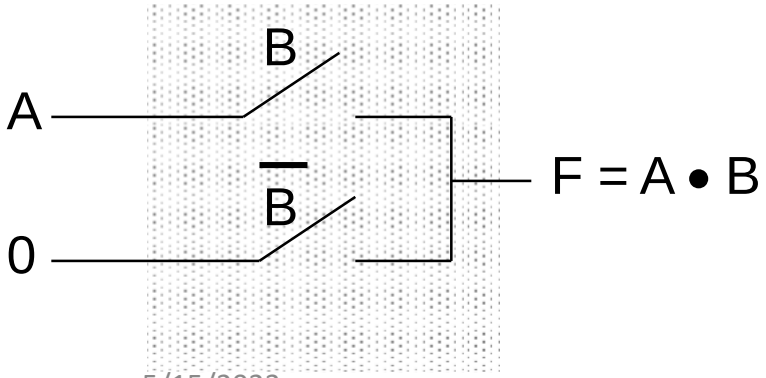
Vout logic levels will be degraded by Vt

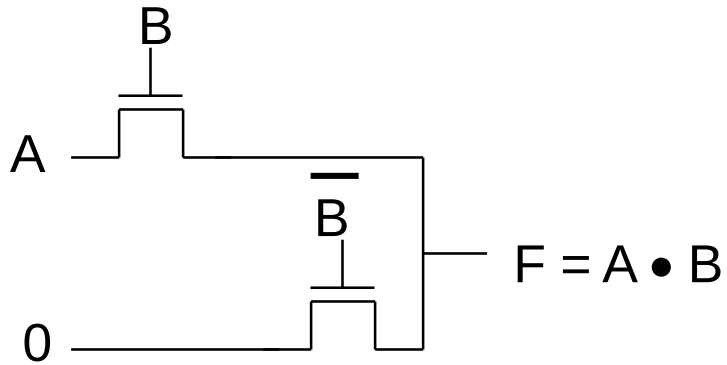


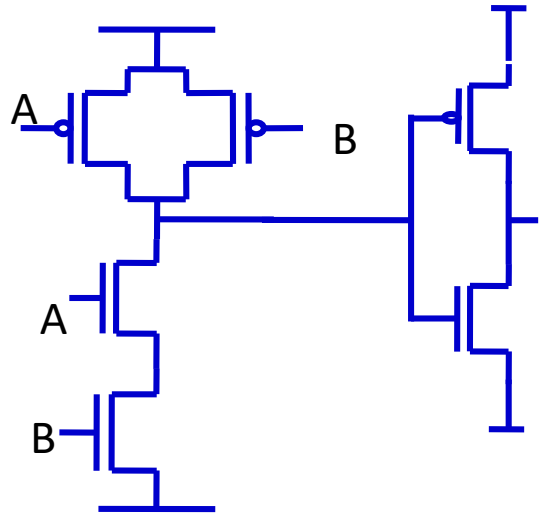
Vout=Vin;
when A,B,C,D,E,F,G,H=1



AND gate with PT logic



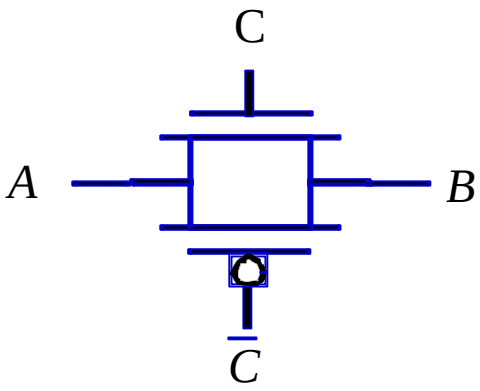


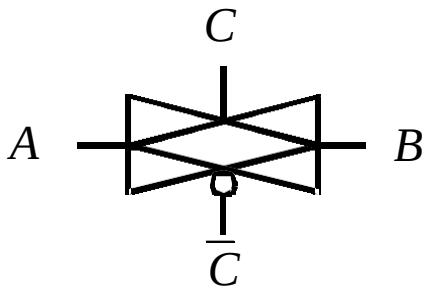


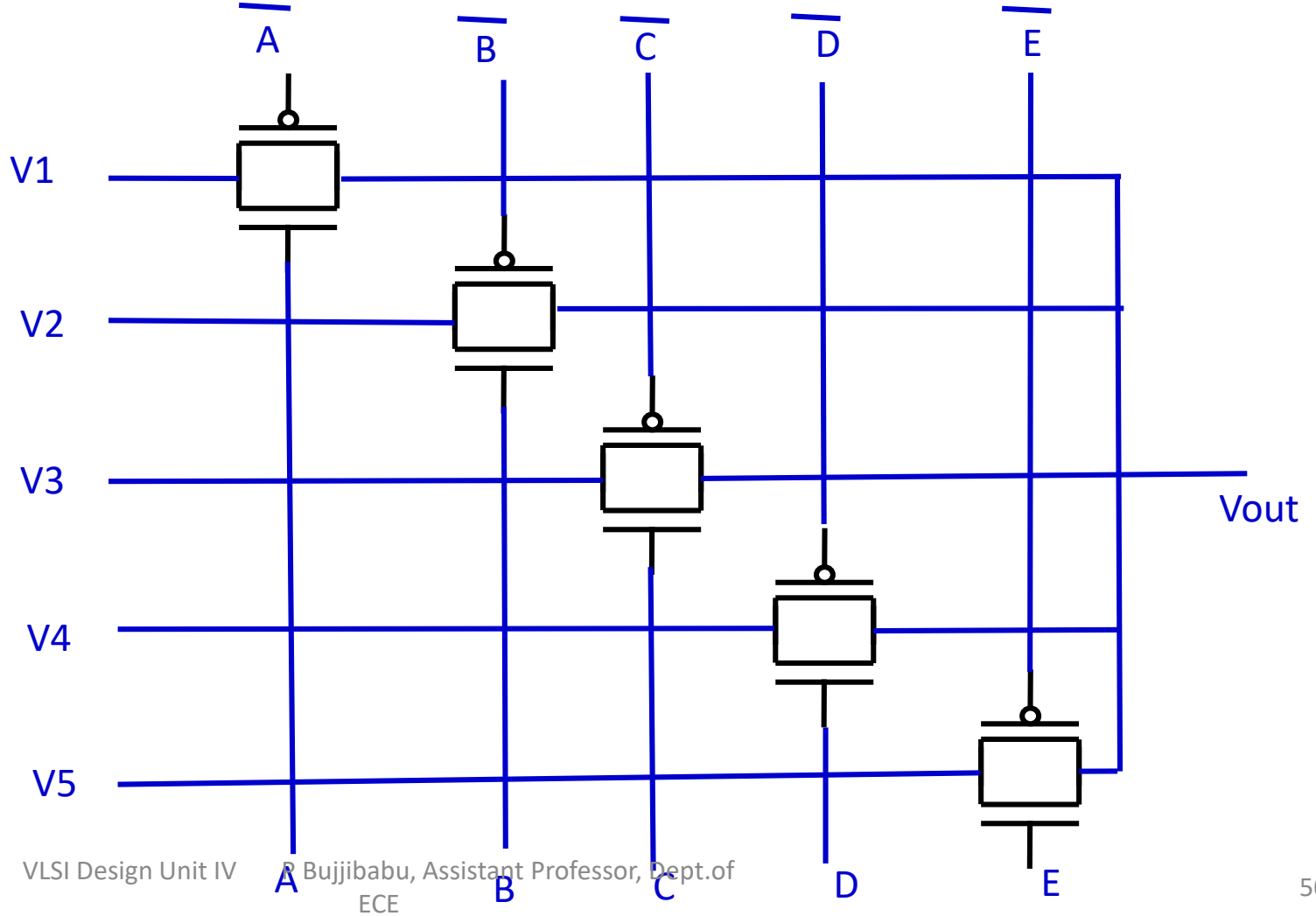
F = A .B

Switch logic & Gate logic: TG logic Examples

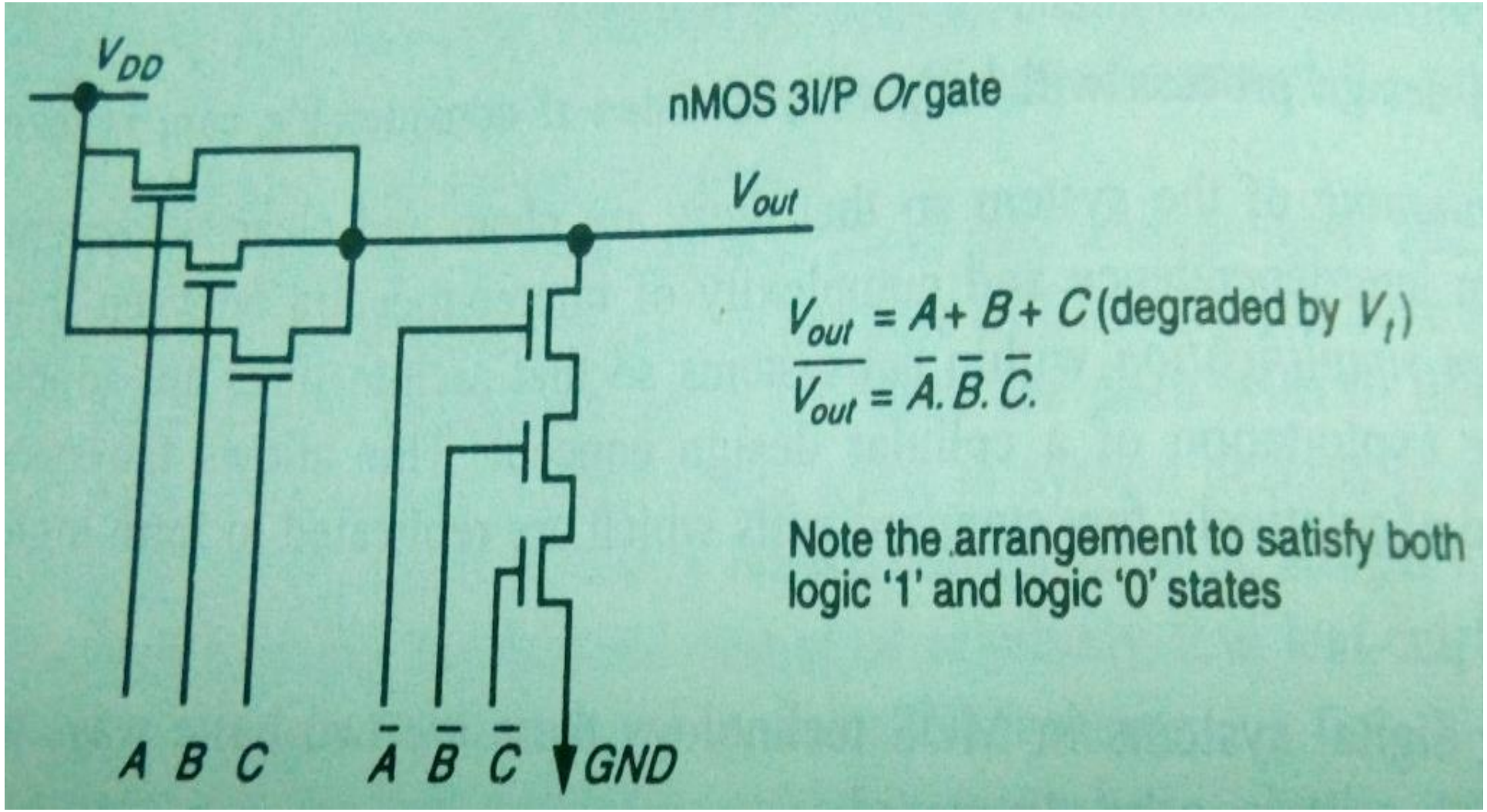
NMOS passes a strong “0” PMOS passes a strong “1”
TG-enable rail-to-rail swing-passes a strong “0” and a strong “1”
These gates are particularly efficient in implementing MUXs



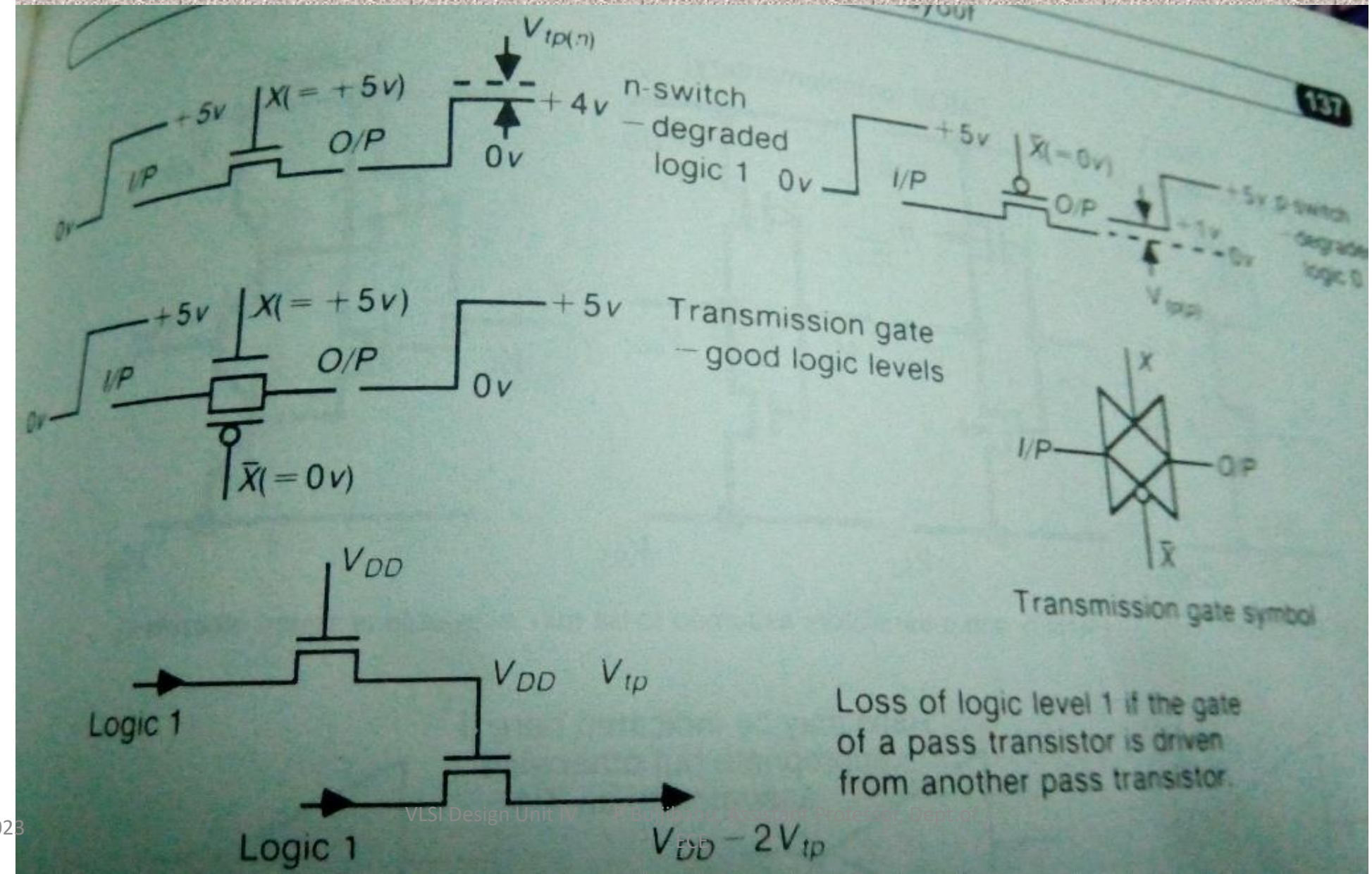




Switch logic & Gate logic



Switch logic & Gate logic

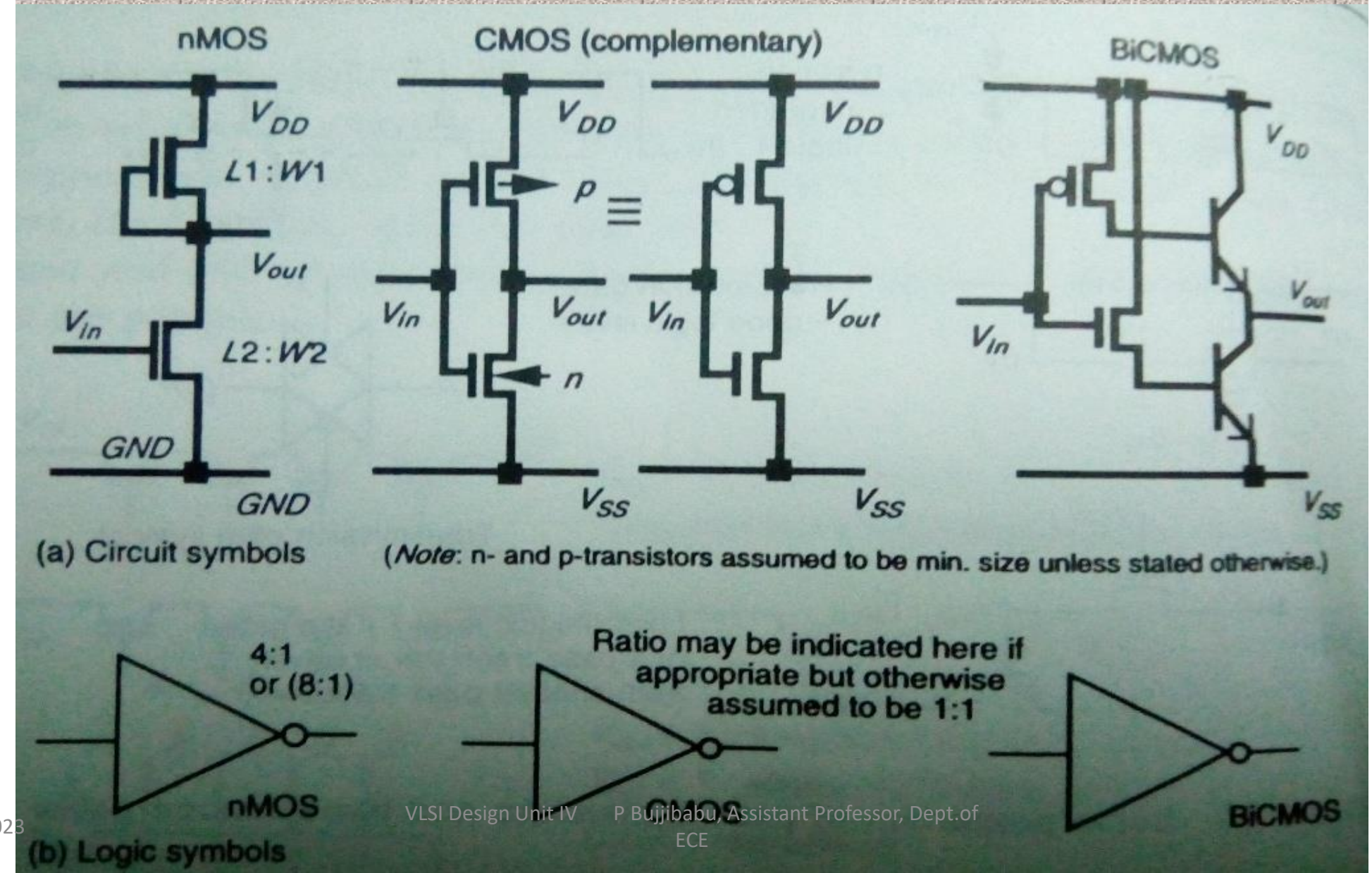


Schematics(different types)can be…

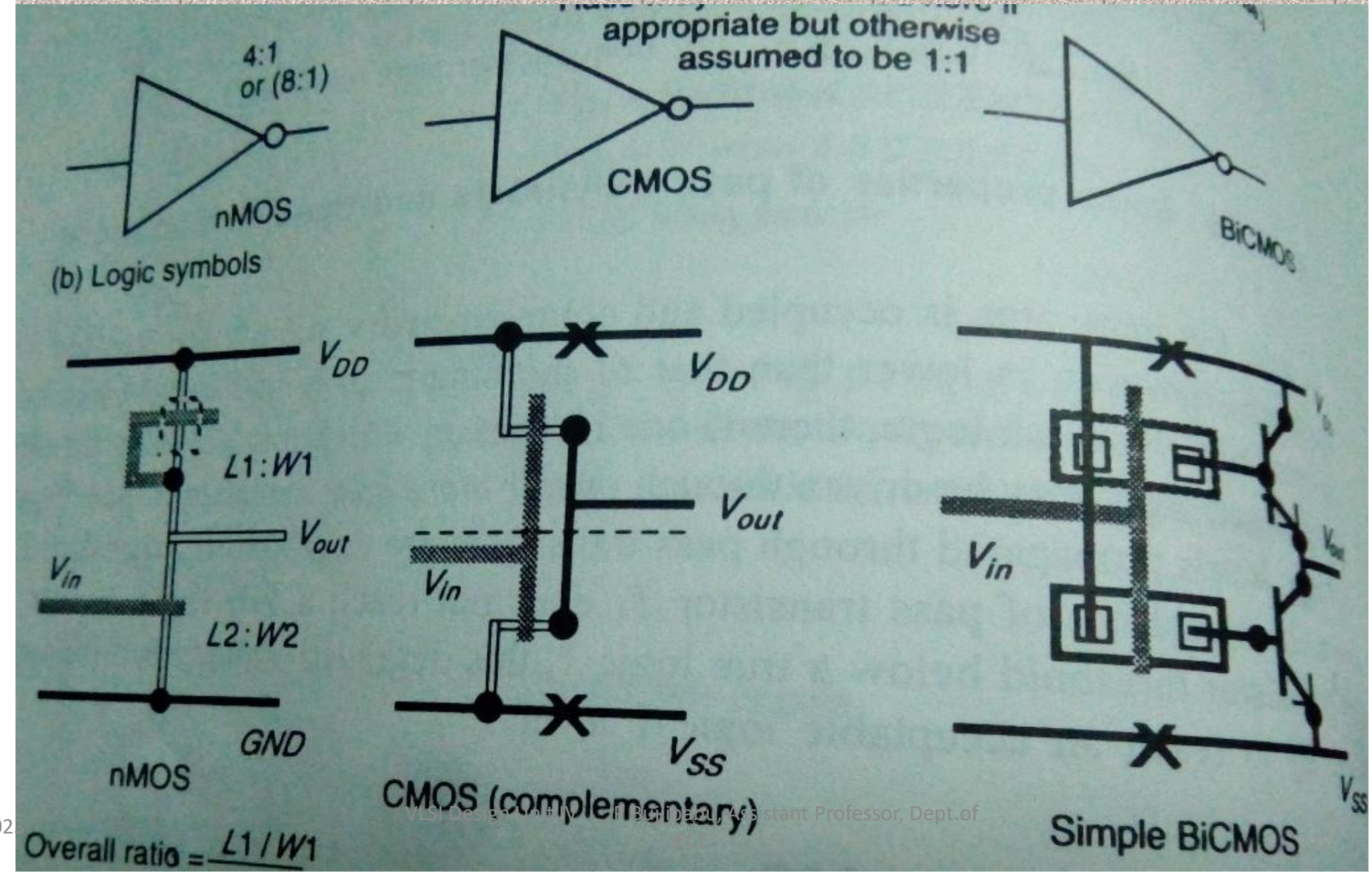
1. Logic with Resistor as PU
2. CMOS Logic
3. Logic with enhancement nMOS as PU
4. Logic with depletion nMOS as PU
5. Pseudo nMOS logic
6. Logic with enhancement pMOS as PD
7. Logic with depletion pMOS as PD
8. Dynamic CMOS Logic
9. Differential Cascade Voltage Switch Logic
10. CMOS Domino Logic
11. GDIL logic
12. Domino logic with pre charge
13. Clocked CMOS Logic (C^2 MOS).
14. NP Domino Logic (Zipper CMOS).
15. Source Follower Pull-up Logic (SFPL).
16. circuits with MTCMOS/VTCMOS logics

No of Transistors changes and area reduces & even power

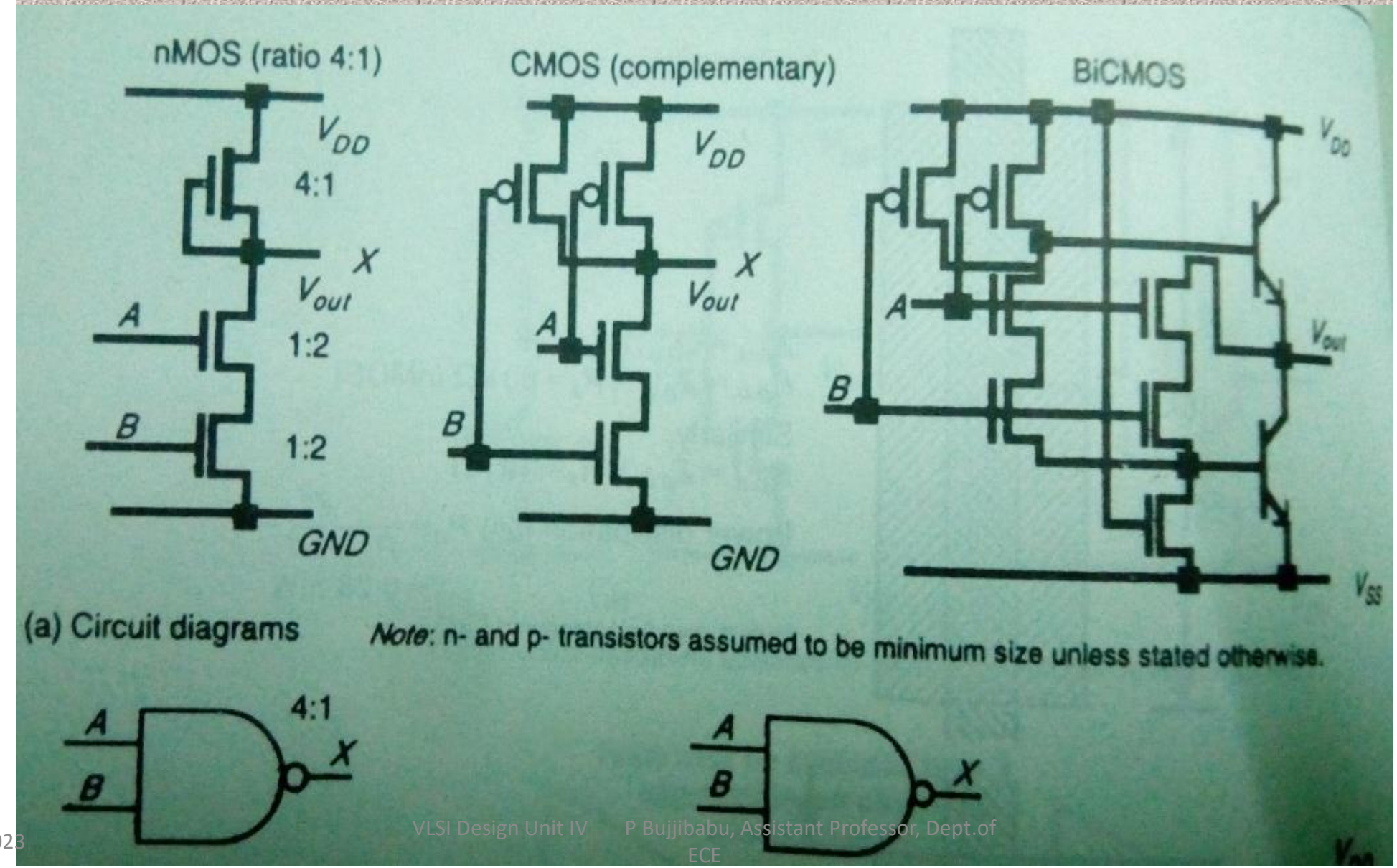
Switch logic & Gate logic



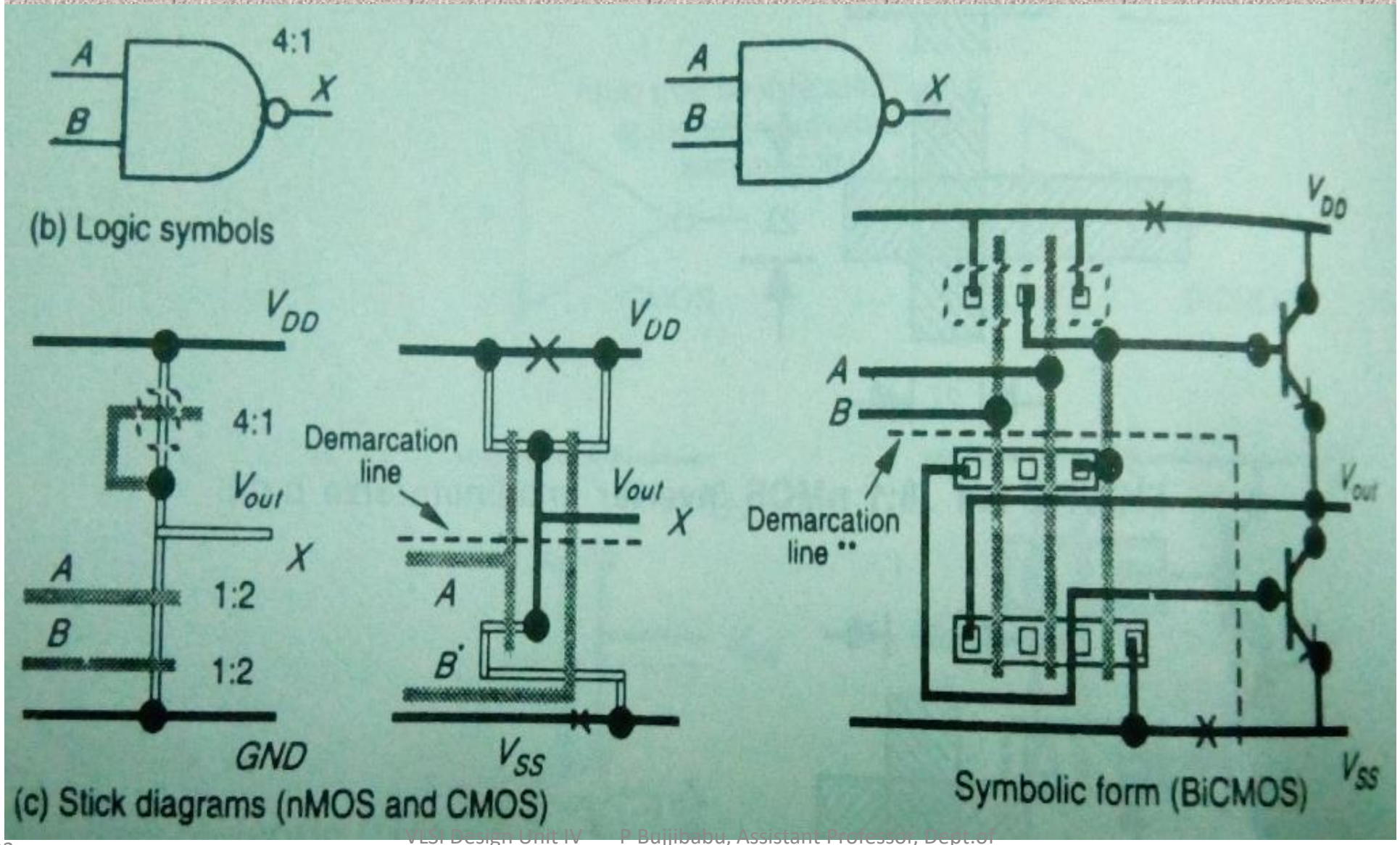
Switch logic & Gate logic



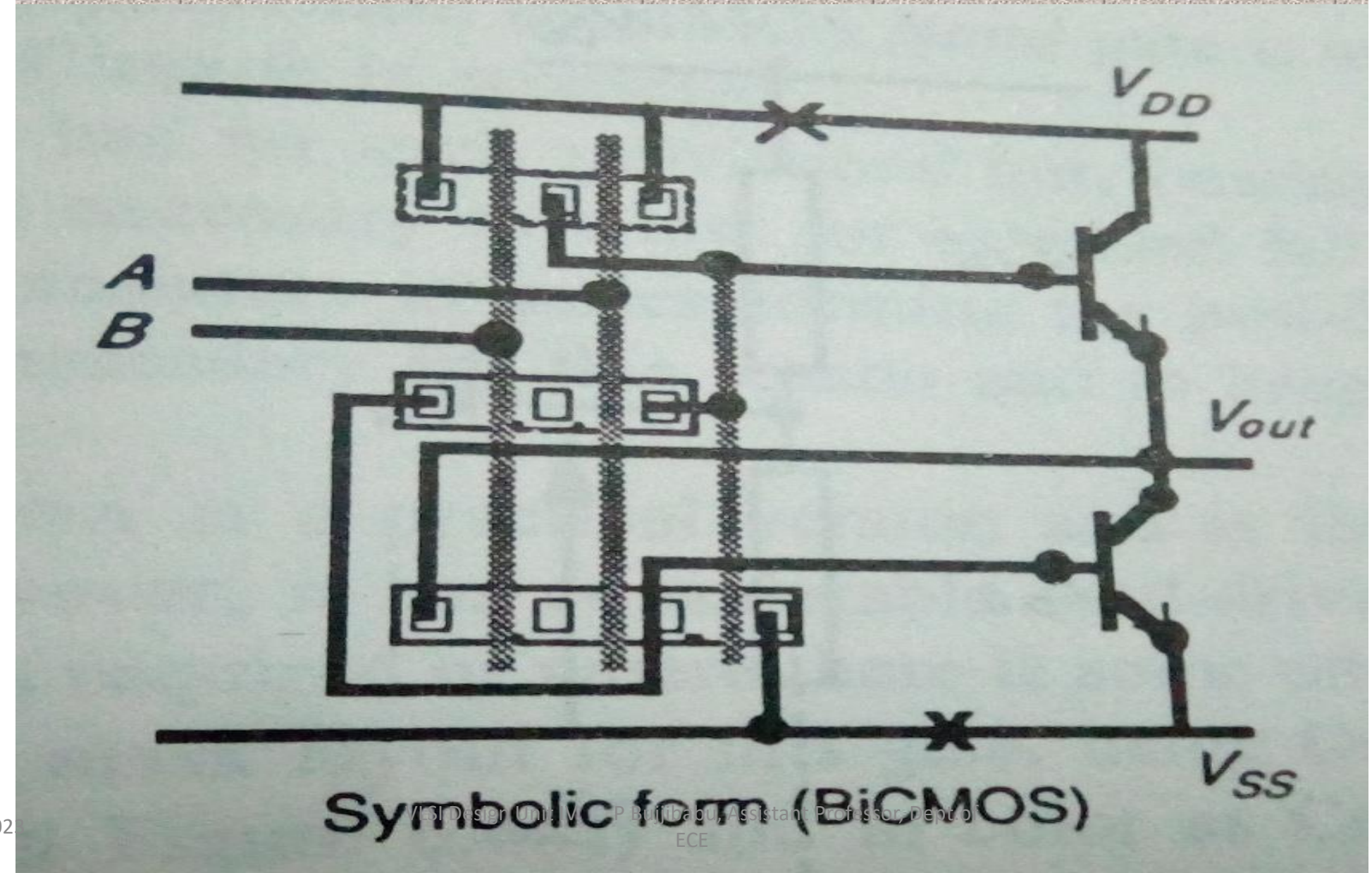
Switch logic & Gate logic



Switch logic & Gate logic

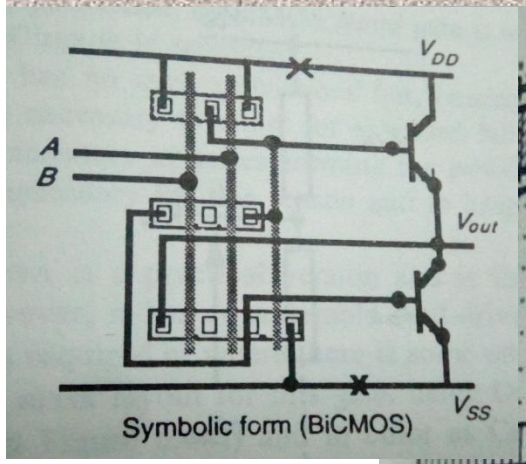


Switch logic & Gate logic

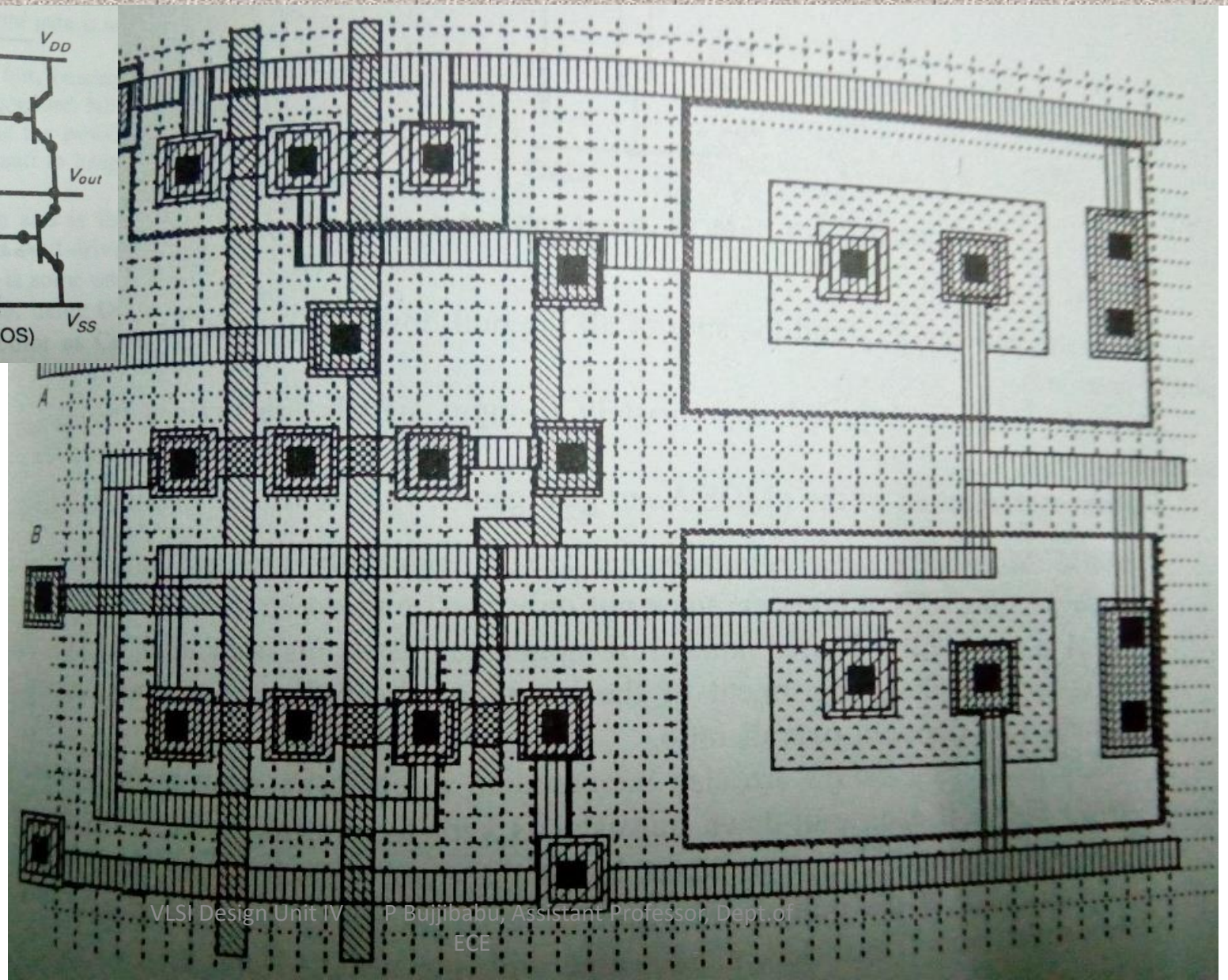


Symbolic form (BiCMOS)

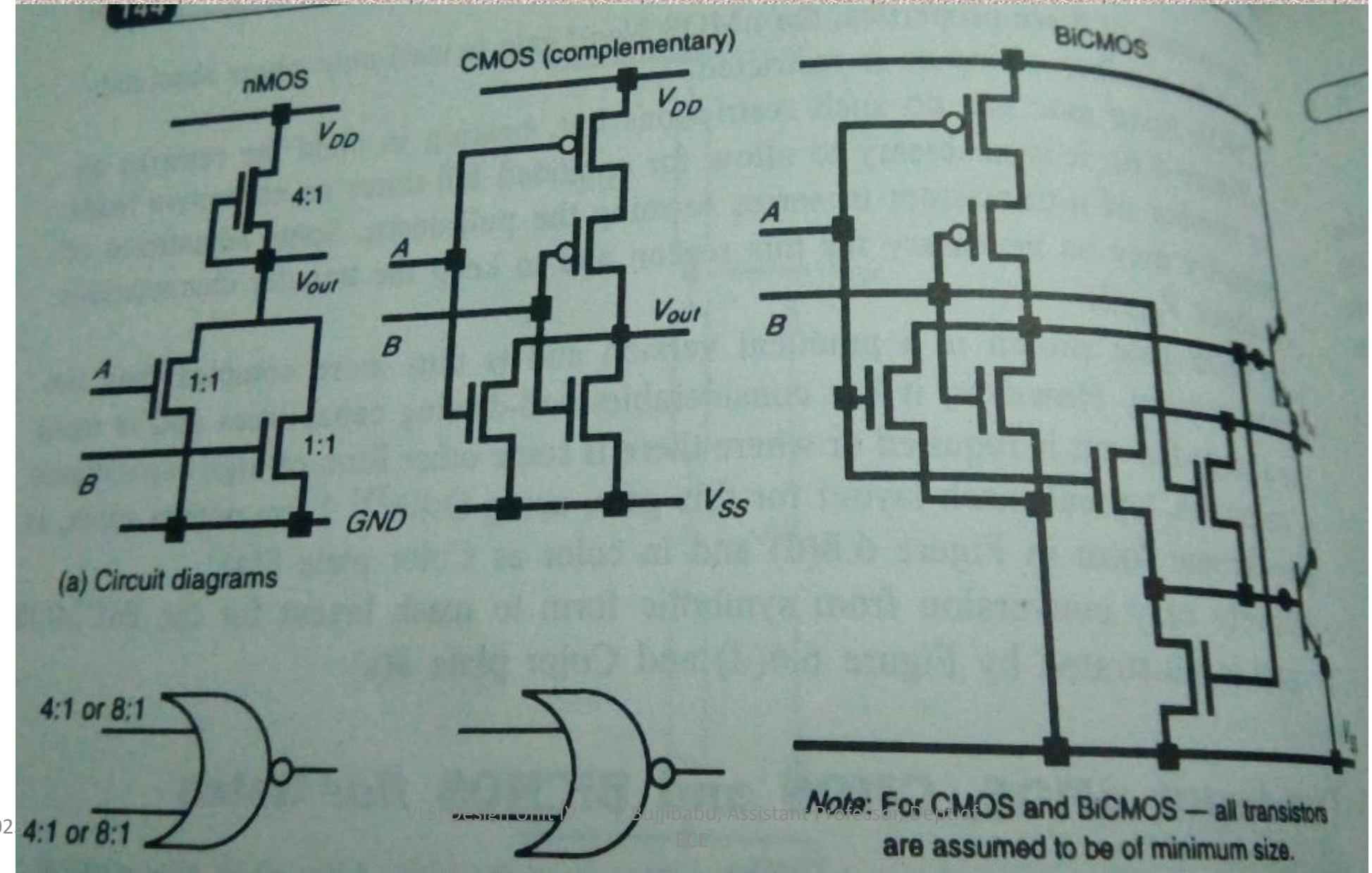
Switch logic & Gate logic



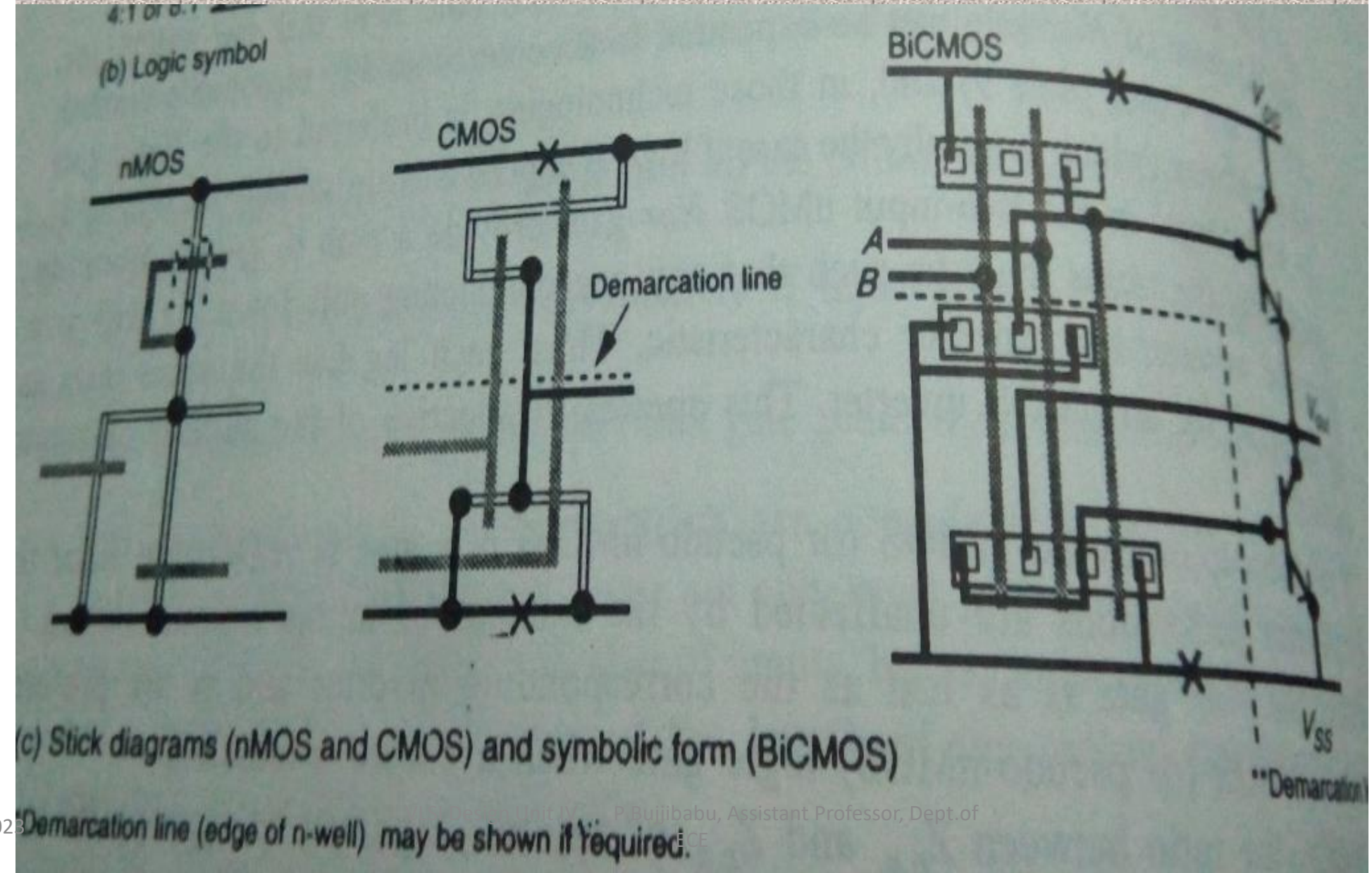
Symbolic form (BiCMOS)



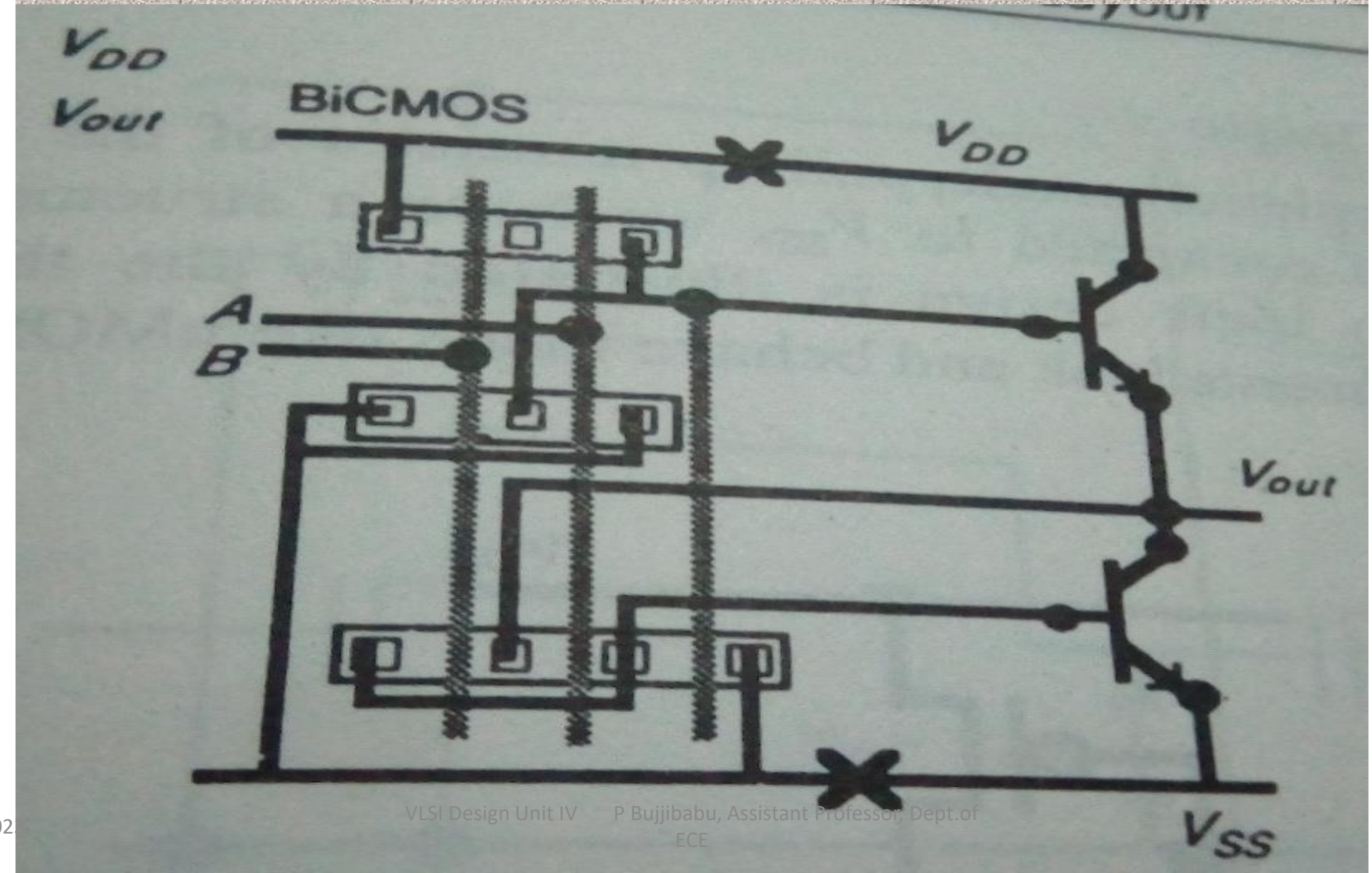
Switch logic & Gate logic



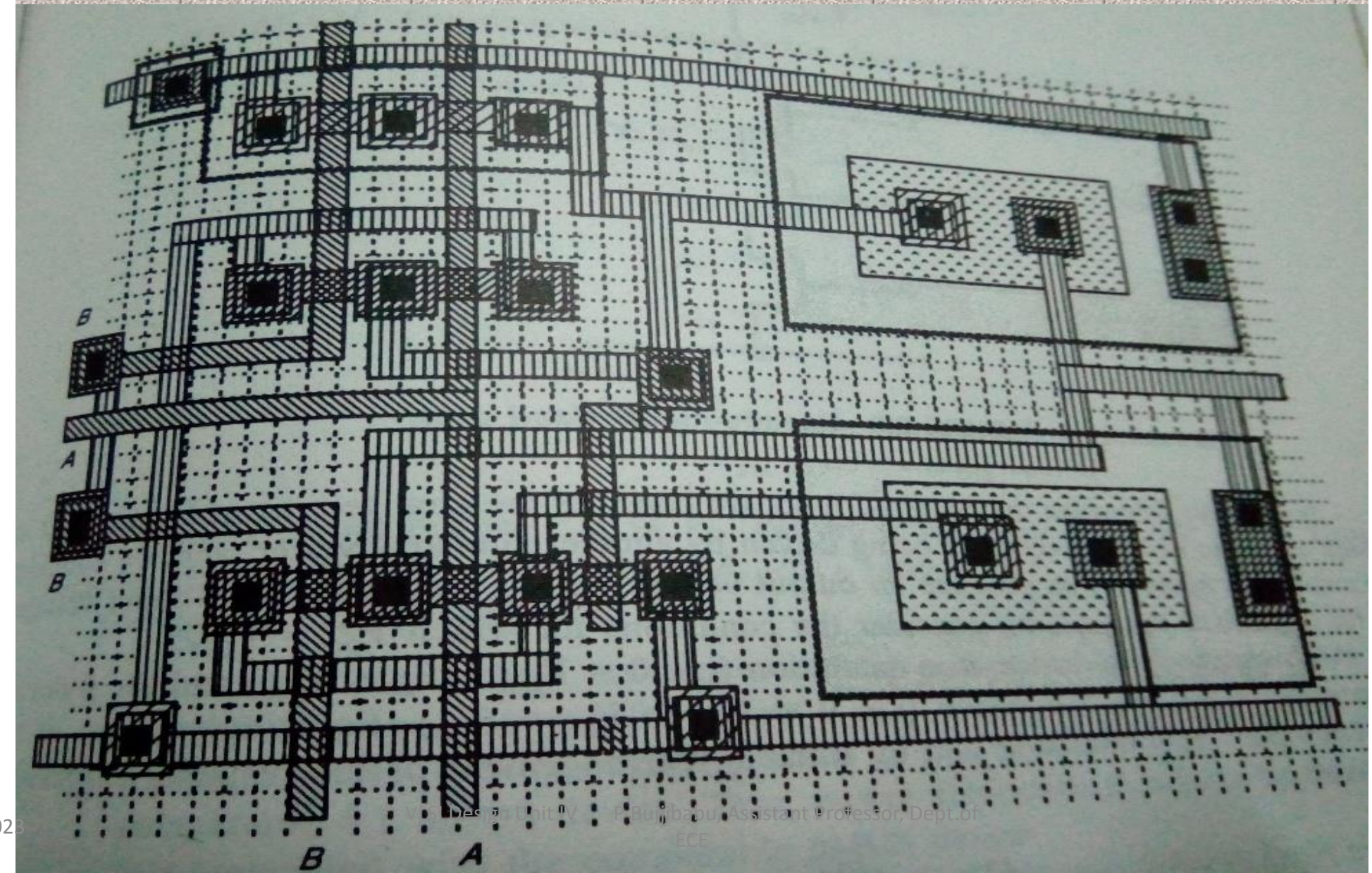
Switch logic & Gate logic



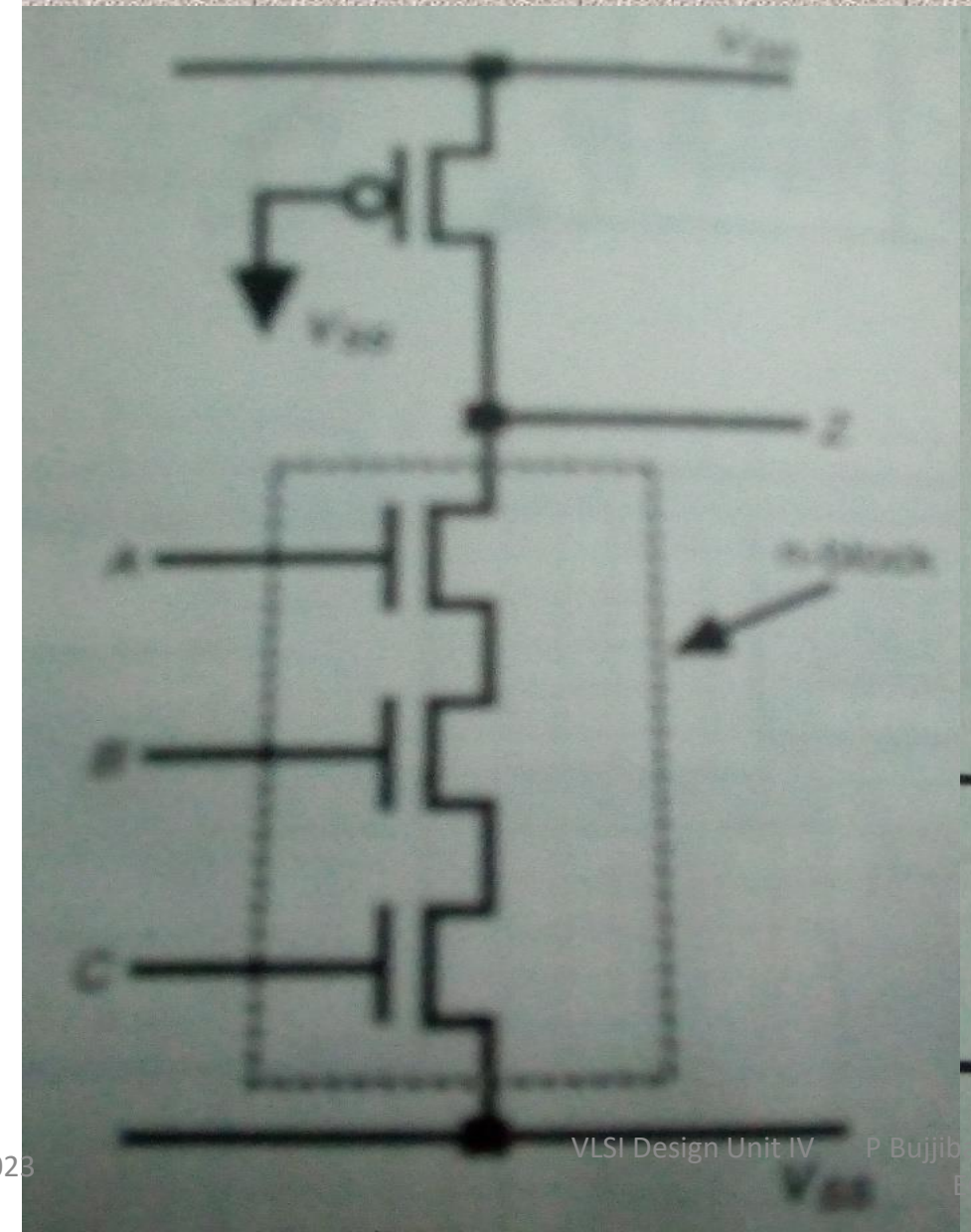
Switch logic & Gate logic

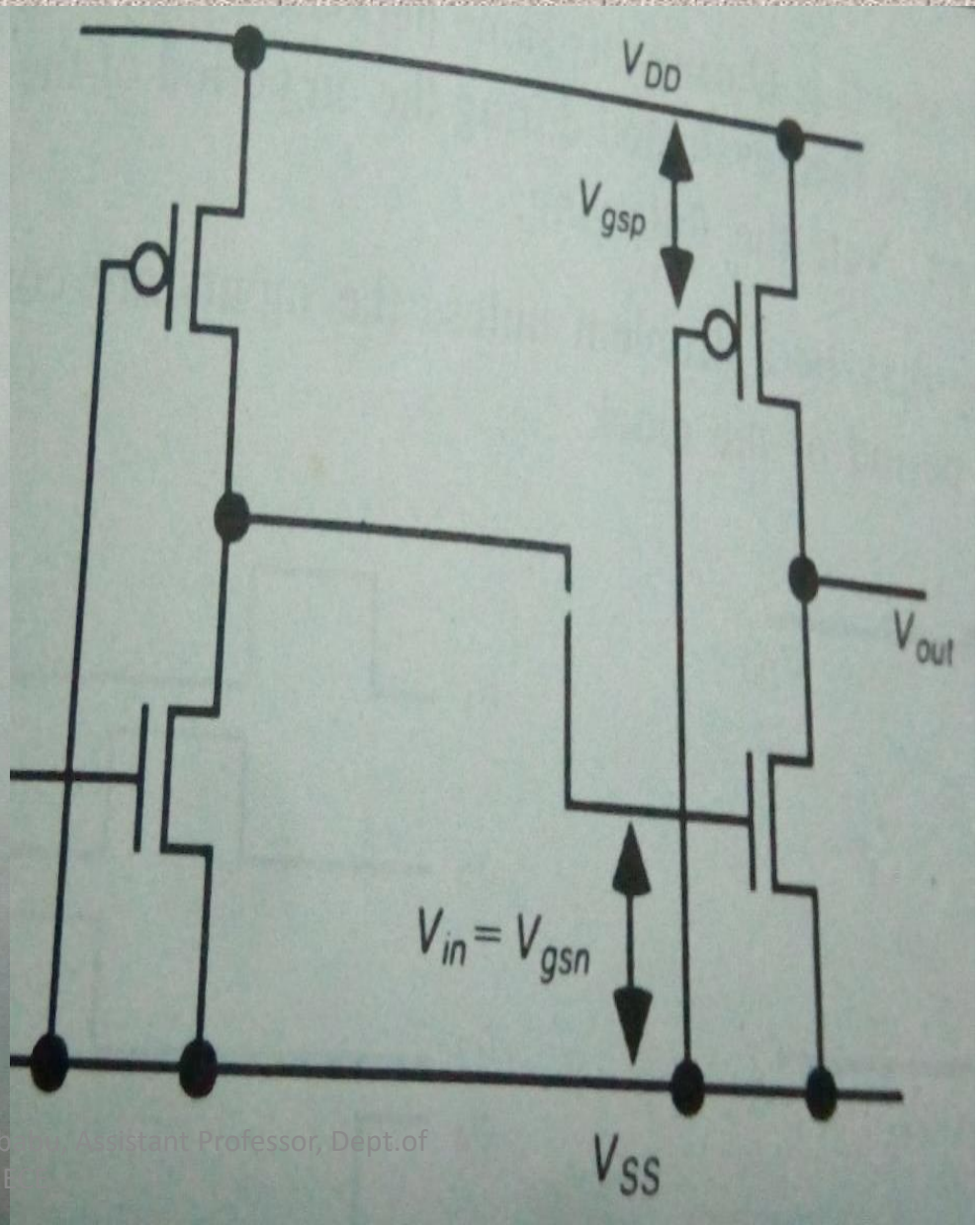


Switch logic & Gate logic

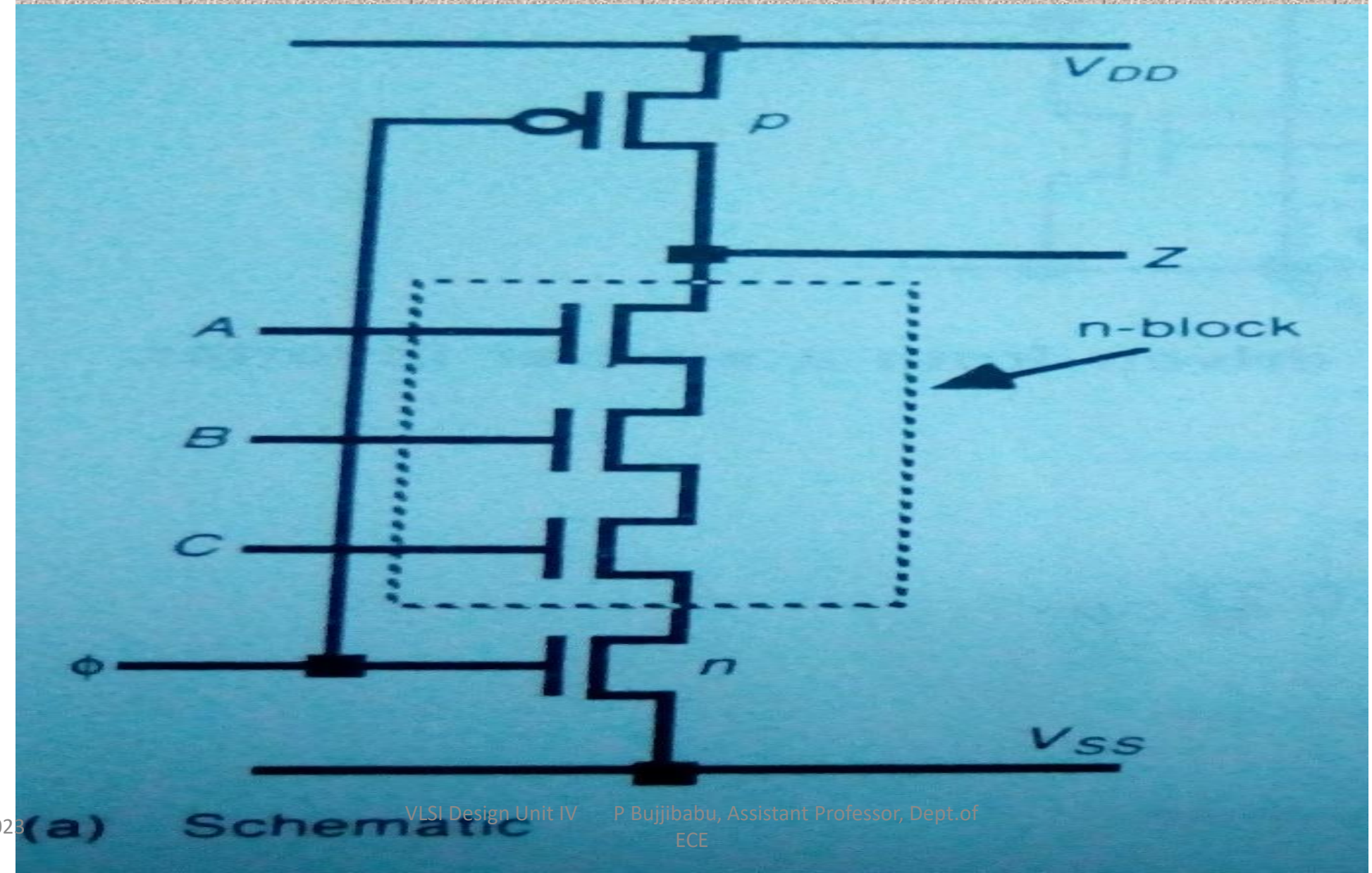


Switch logic & Gate logic

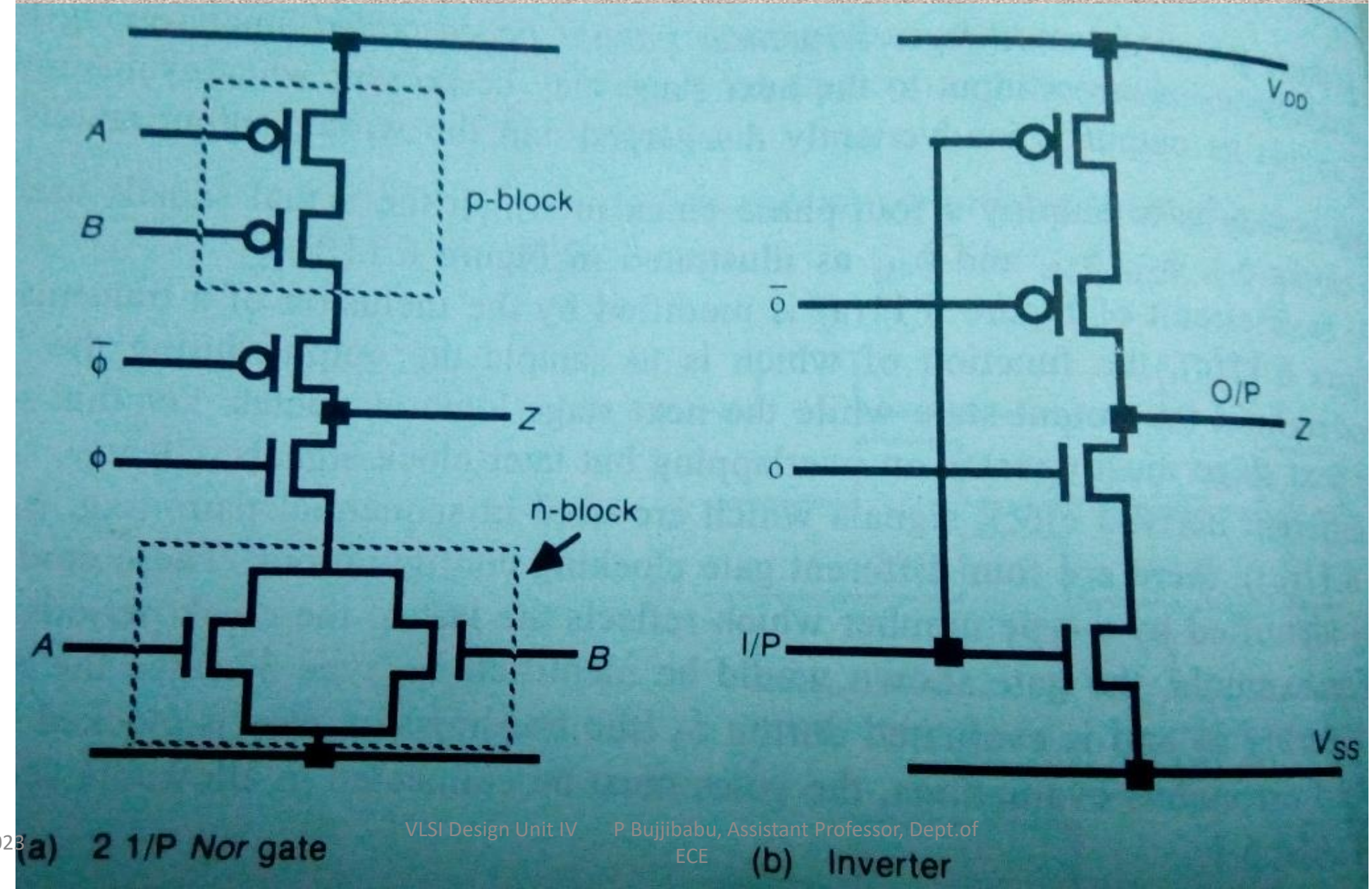




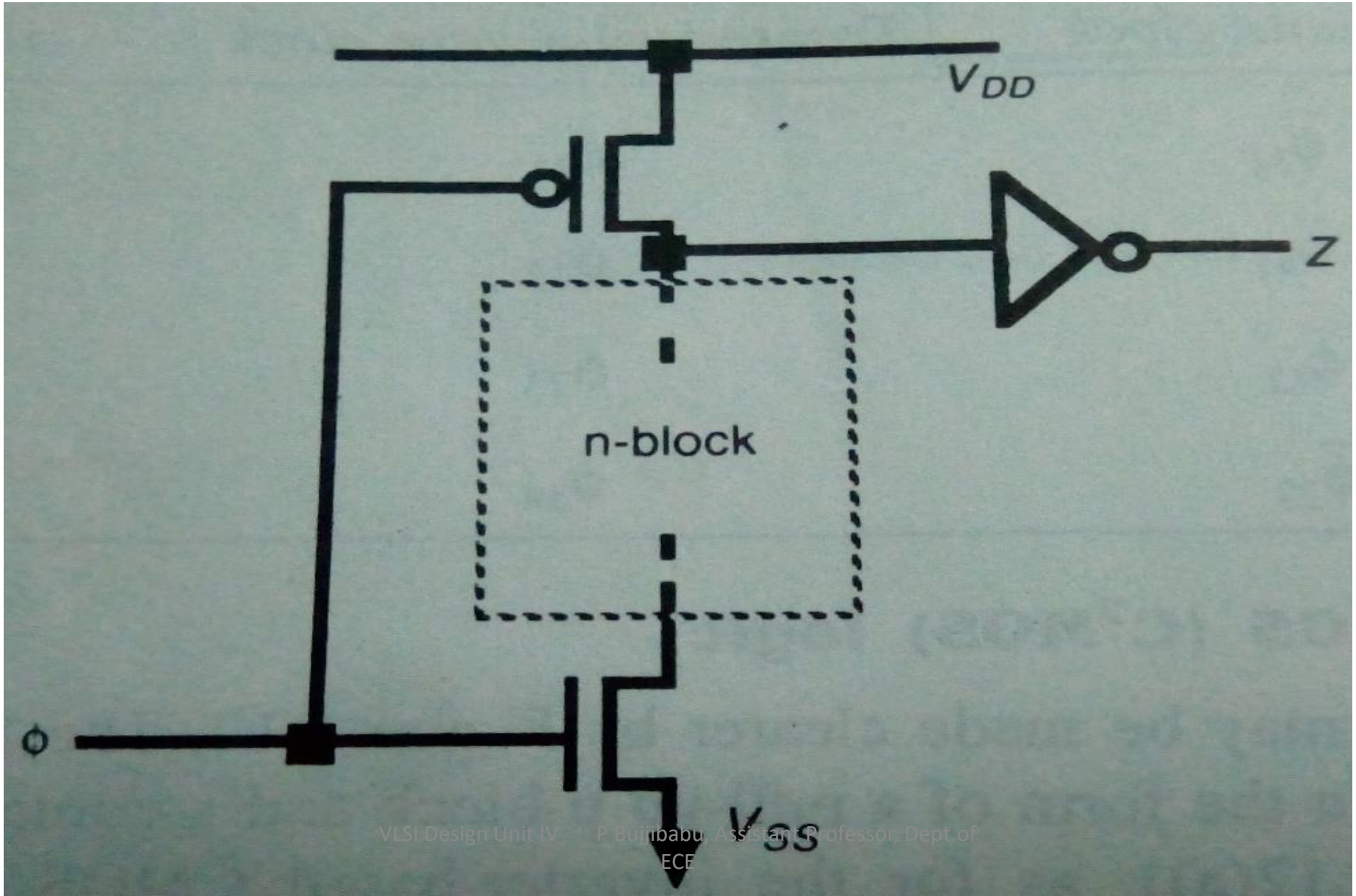
Switch logic & Gate logic



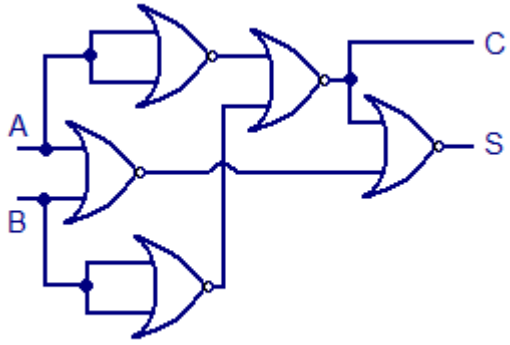
Gate logic: Clocked CMOS logic



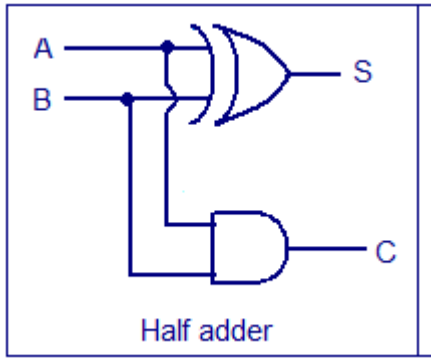
Gate logic: Domino logic



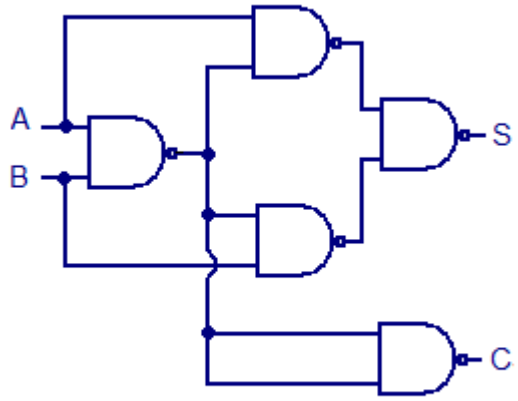
Examples of structured design, Adder RTL diagrams



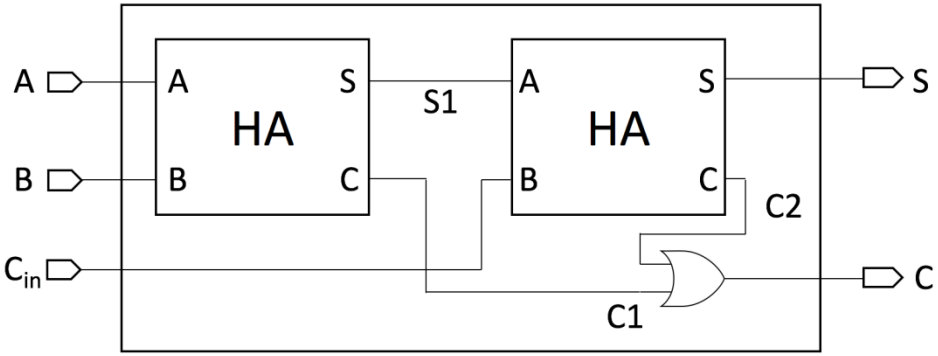
Half adder using NOR logic

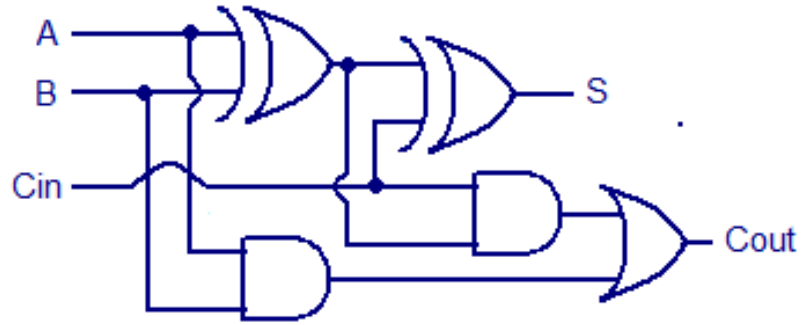


Half adder

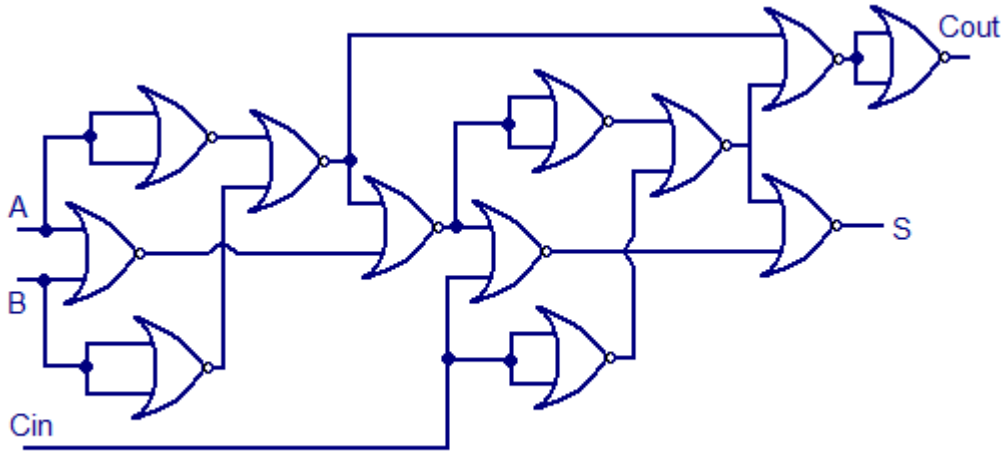


Half adder using NAND logic

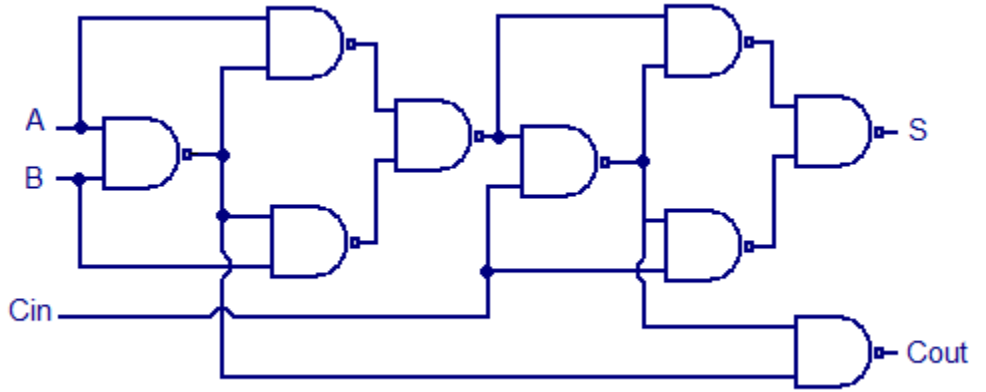




Full adder



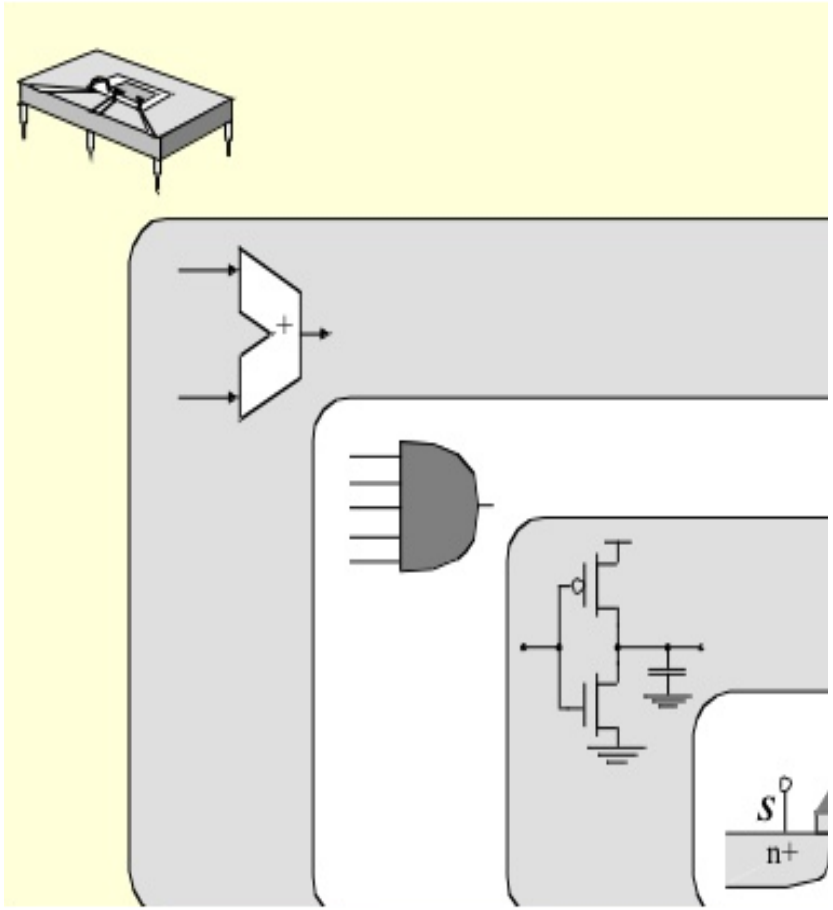
Full adder using NOR logic

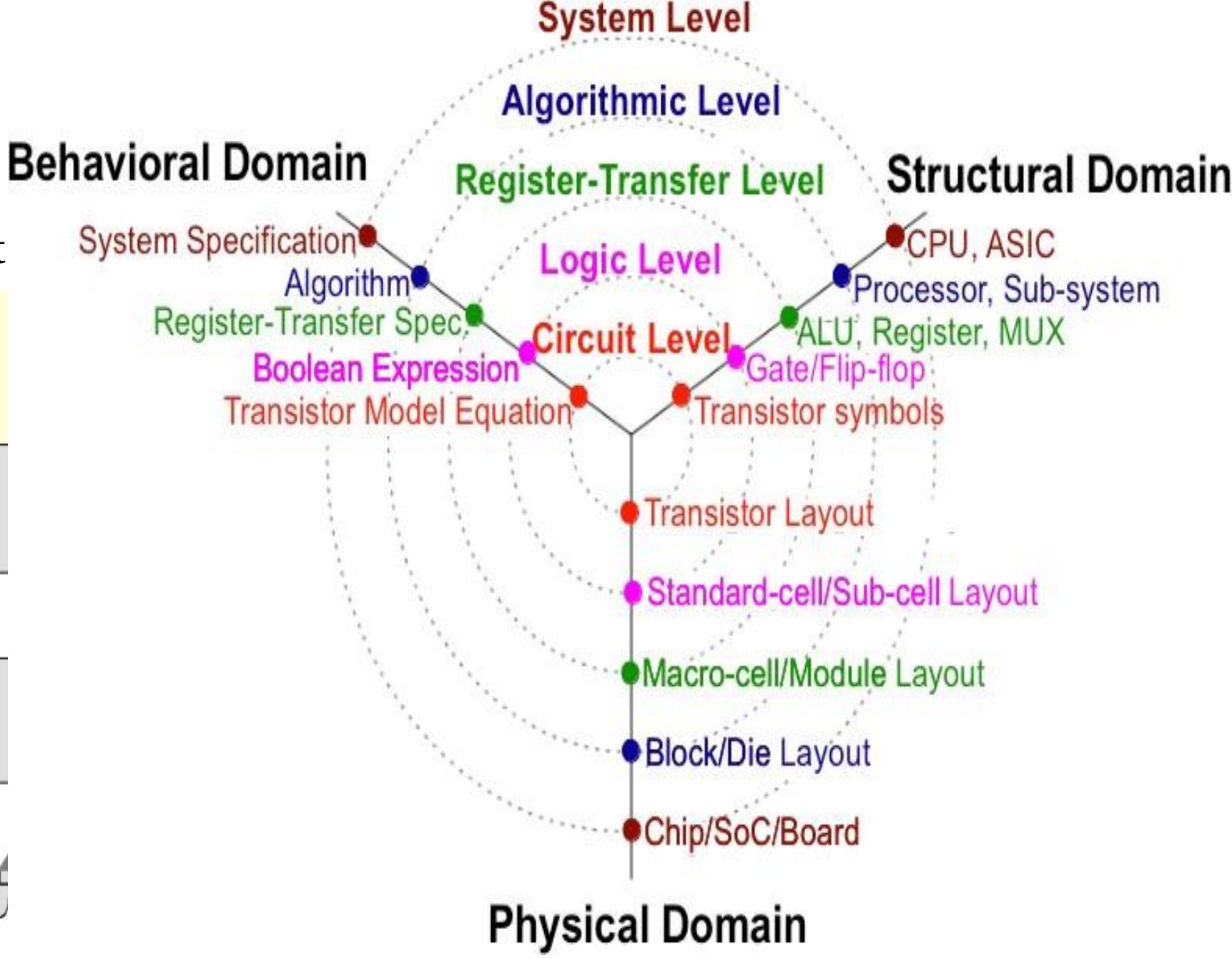


Full adder using NAND logic

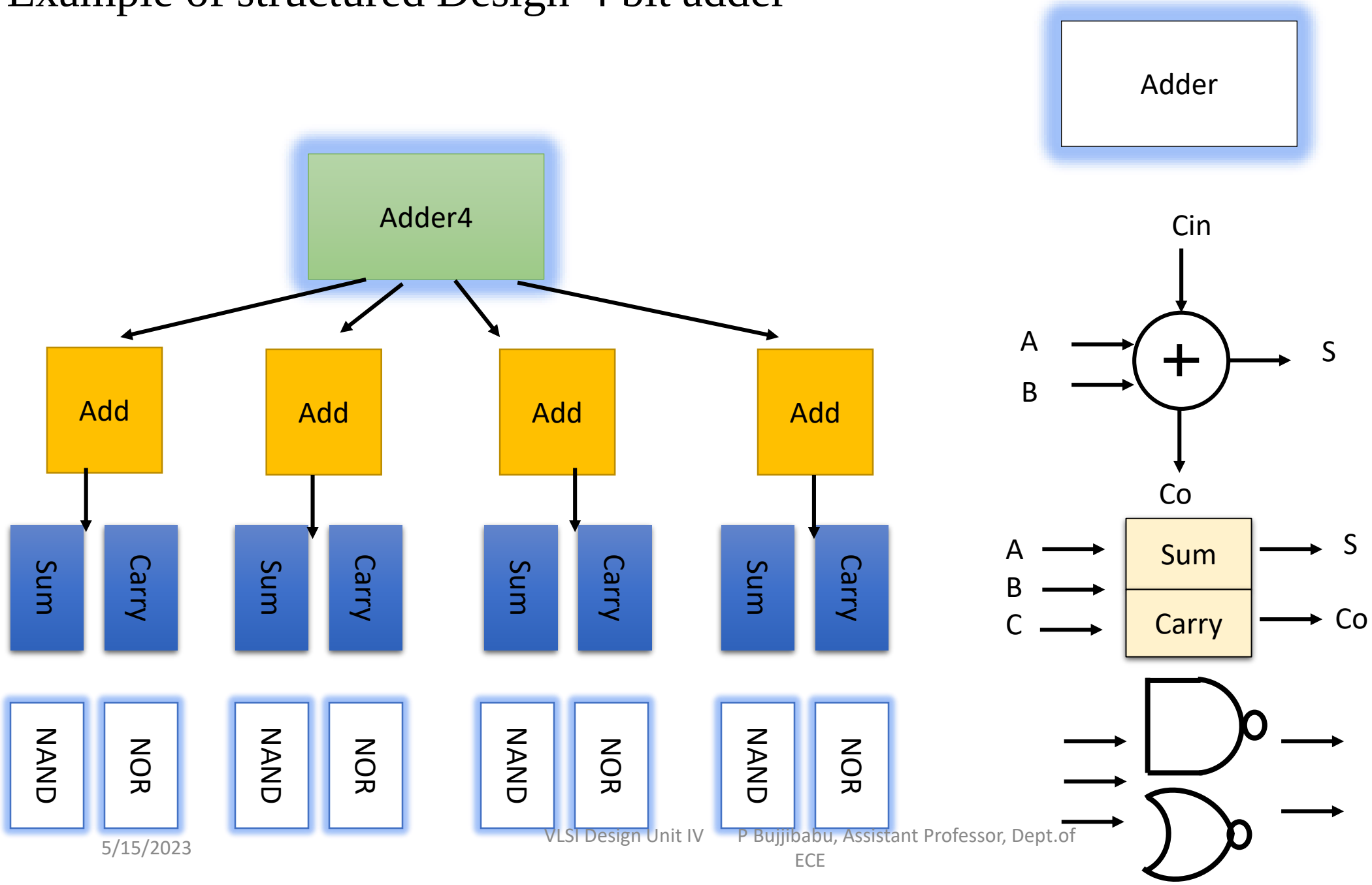
Structured Design

- Levels of abstraction-Y chart

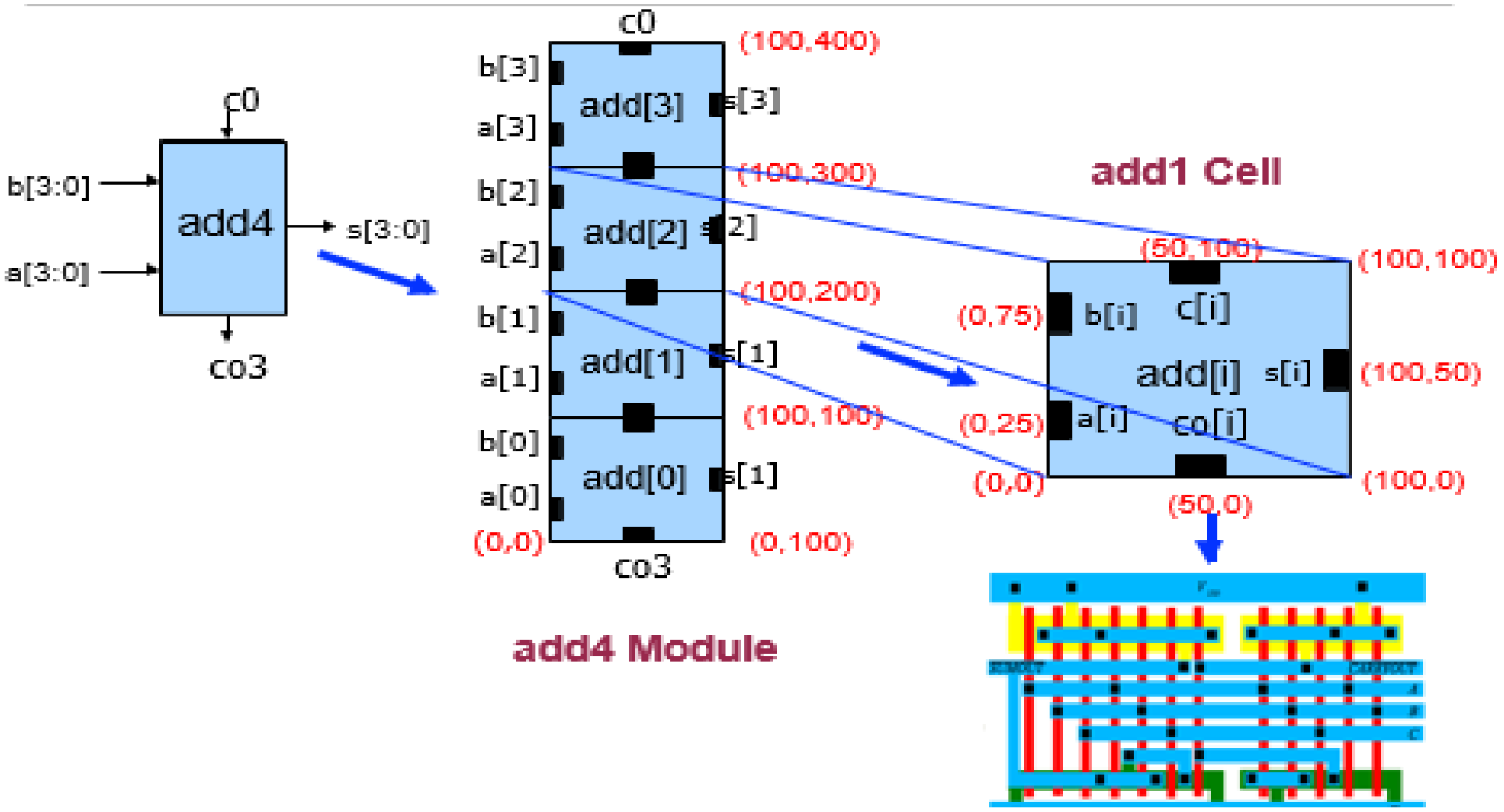




Example of structured Design-4 bit adder



Hierarchical & Modular Layout



Example of structured Design

Design Strategies:

- Metrics for Design Success:
  - Performance Specs
    - logical function, speed, power, area
  - Time to Design
    - engineering cost and schedule
  - Ease of Test Generation and Testability
    - engineering cost, manufacturing cost, schedule
- Design is a continuous tradeoff to achieve performance specs with adequate results in the other metrics
- **Hierarchy:** Subdivide the design in several levels of sub- modules
- **Modularity:** Define sub-modules unambiguously and well defined interfaces
- **Regularity:** Subdivide to max number of similar sub- modules at each level
- **Locality:** Max local connections, keeping critical paths within module boundaries

Examples of structured Design

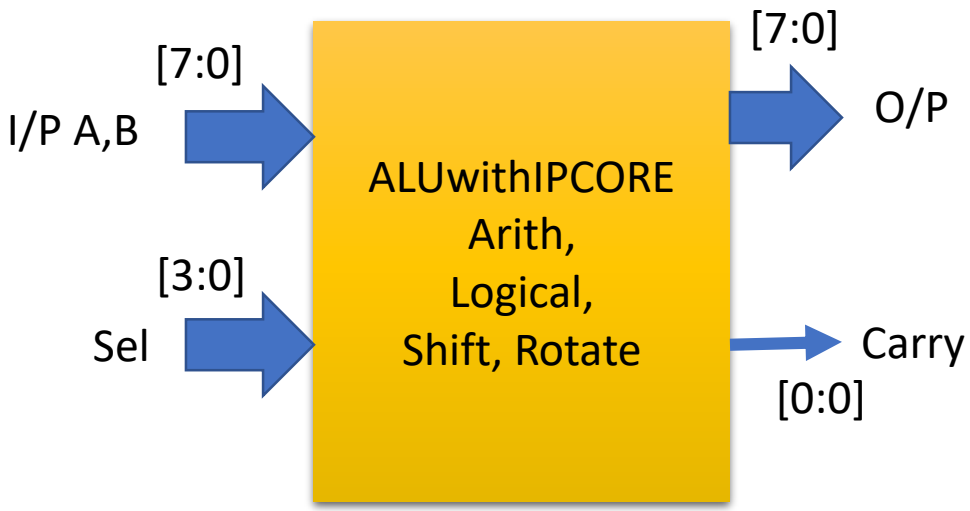
ALU

Parity Generator(or xor gate)

Bus arbitration logic- or control logic

Ect…

An illustration of Design process: ALU



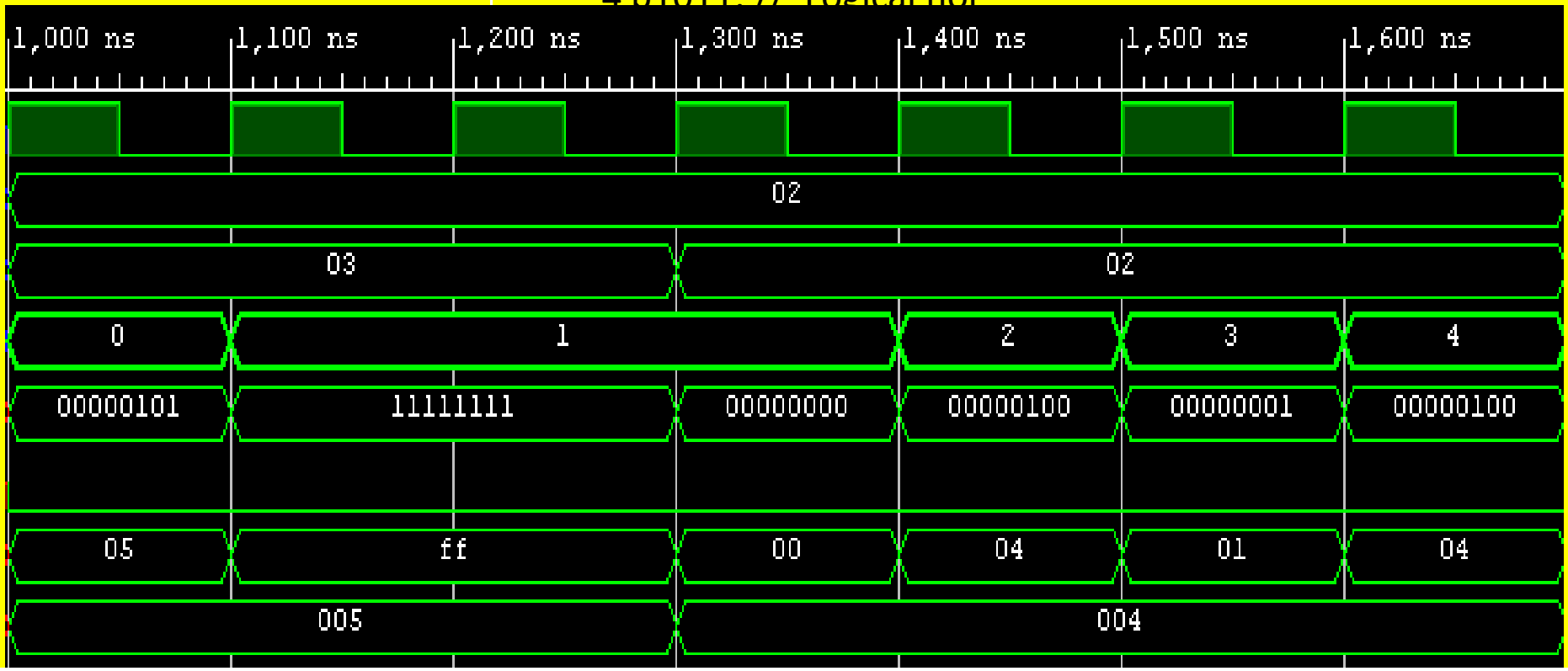

```
module ALUwithIPCORE(
        input [7:0] A,B,  // ALU 8-bit Inputs
        input [3:0] ALU_Sel,// ALU Selection
        output [7:0] ALU_Out, // ALU 8-bit Output
        output CarryOut // Carry Out Flag
       );

   reg [7:0] ALU_Result;
   wire [8:0] tmp;
   assign ALU_Out = ALU_Result; // ALU out
   assign tmp = {1'b0,A} + {1'b0,B};
   assign CarryOut = tmp[8]; // Carryout flag
```

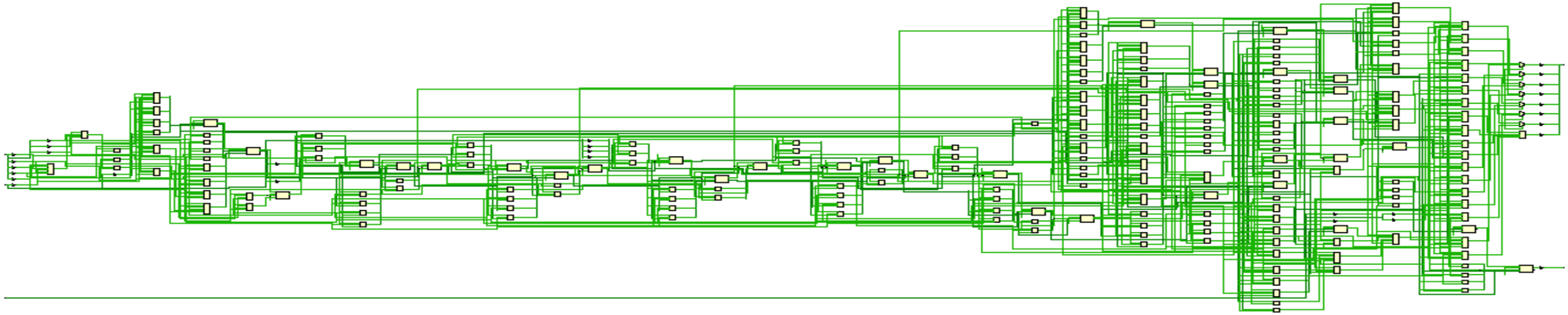
An illustration of Design process: ALU

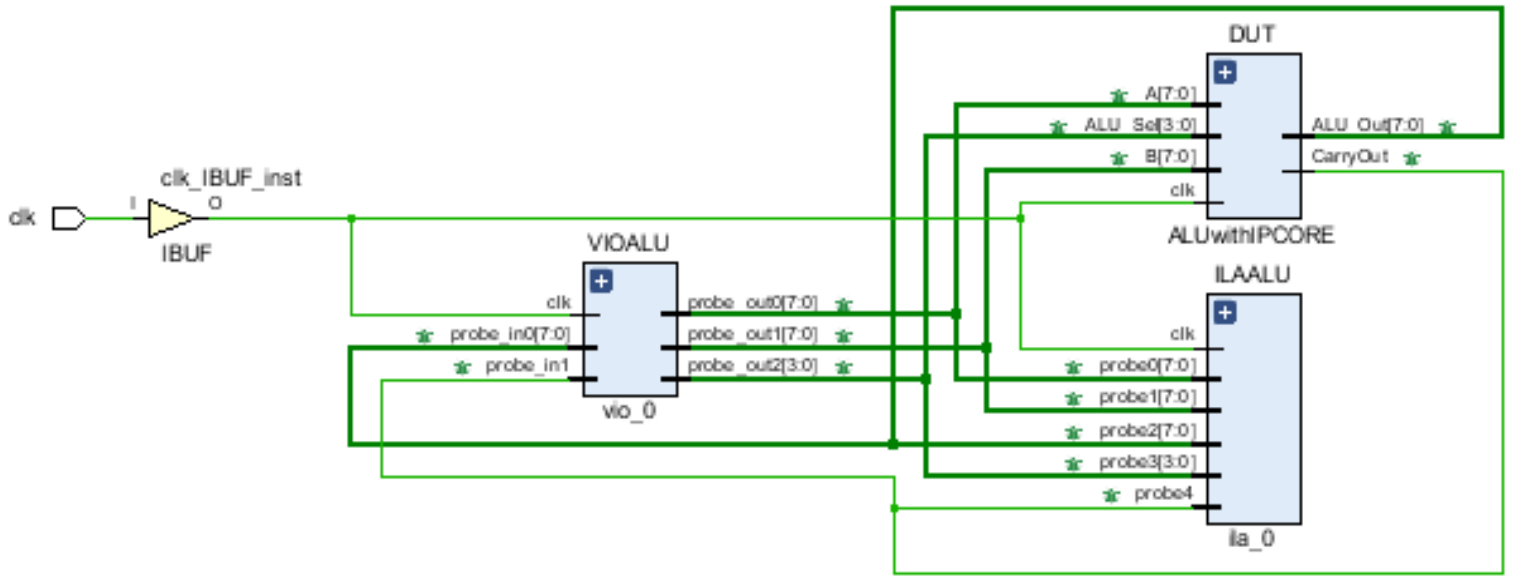
```
always @(*)
   begin
      case(ALU_Sel)
      4'b0000: // Addition
        ALU_Result = A + B ;
      4'b0001: // Subtraction
        ALU_Result = A - B ;
      4'b0010: // Multiplication
        ALU_Result = A * B;
      4'b0011: // Division
        ALU_Result = A/B;
      4'b0100: // Logical shift left
       ALU_Result = A<<1;
      4'b0101: // Logical shift right
        ALU_Result = A>>1;
       4'b0110: // Rotate left
        ALU_Result = {A[6:0],A[7]};
       4'b0111: // Rotate right
        ALU_Result = {A[0],A[7:1]};
```

```
      4'b1000: //  Logical and
       ALU_Result = A & B;
      4'b1001: //  Logical or
       ALU_Result = A | B;
      4'b1010: //  Logical xor
       ALU_Result = A ^ B;
      4'b1011: //  Logical nor
```

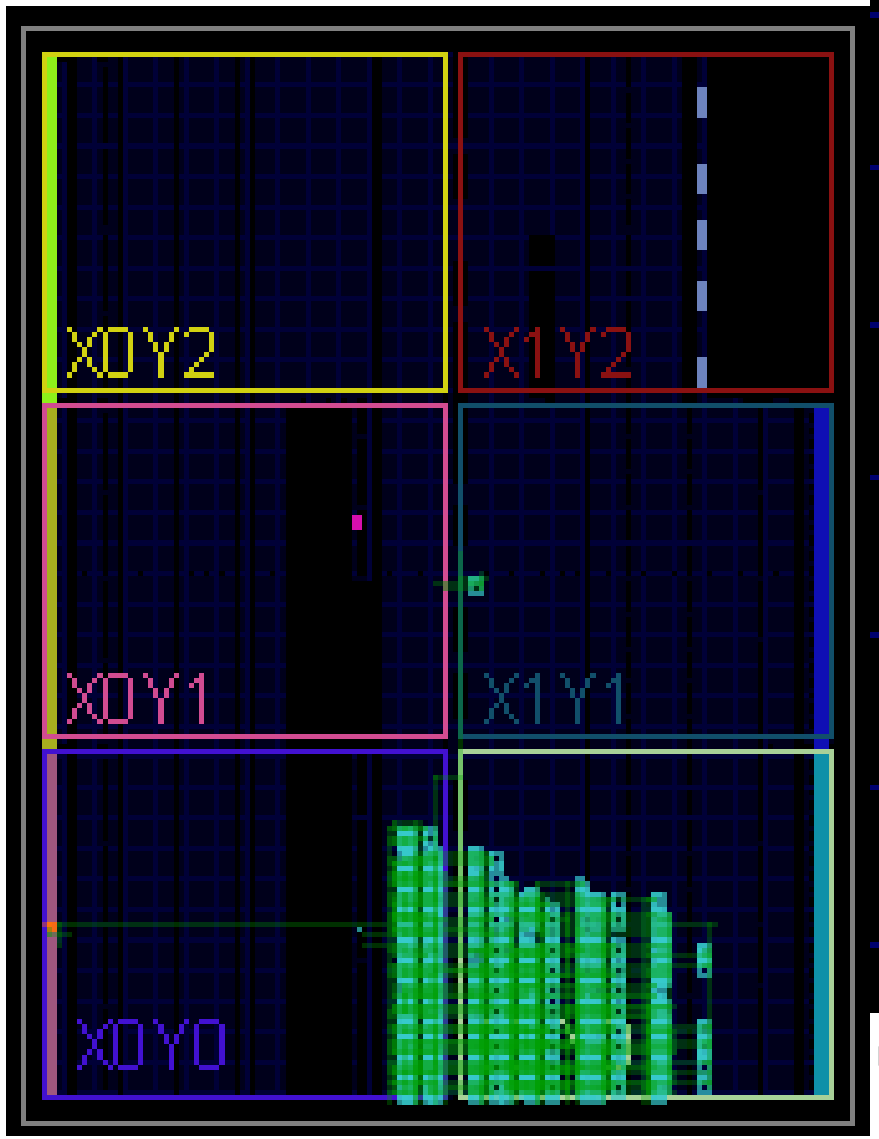


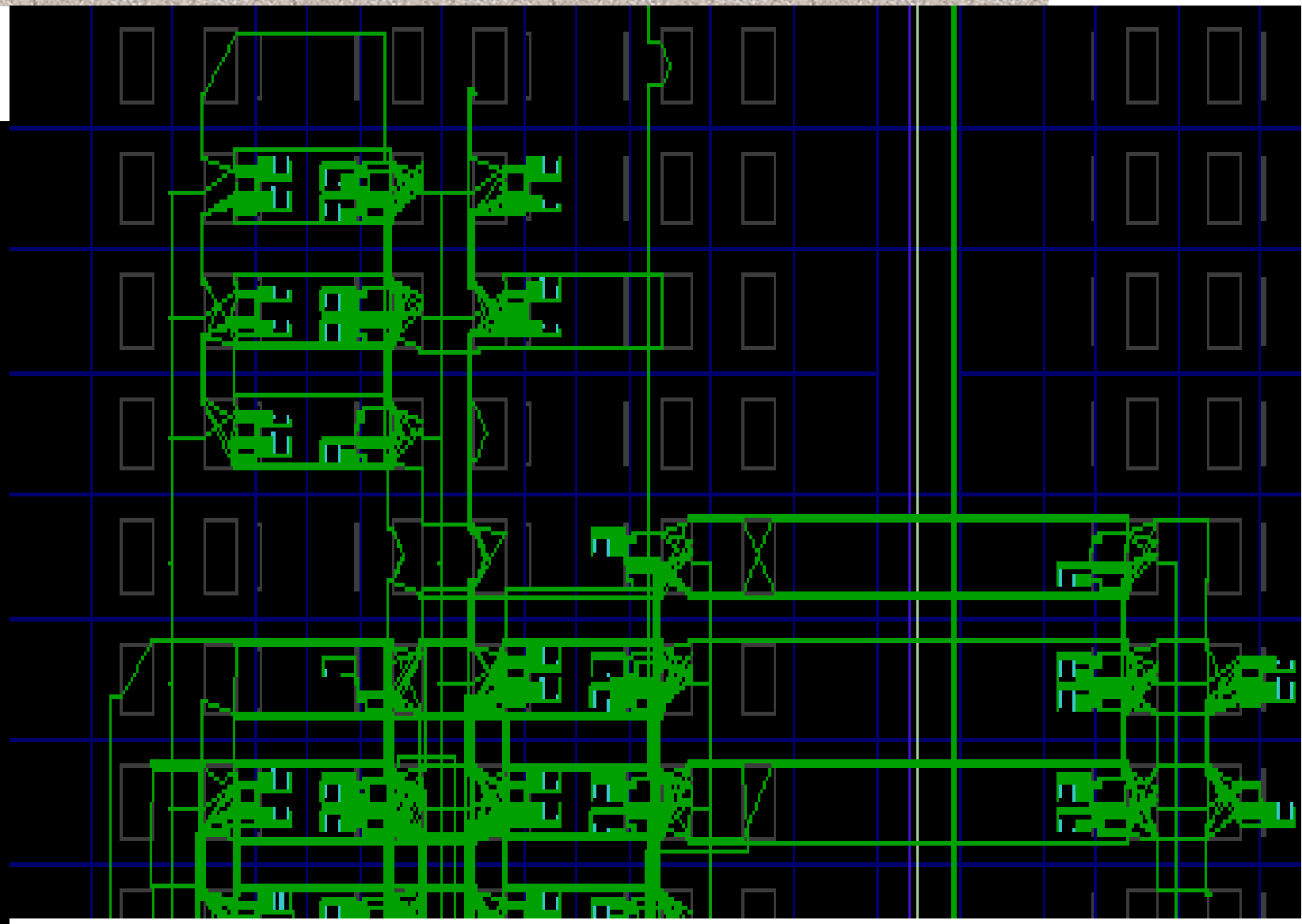
An illustration of Design process: ALU





An illustration of Design process: ALU





Working with FPGA-With the core

In a case, where total number of input/output pins are very high(not possible to observe the output without additional modules) then the core usage is required.

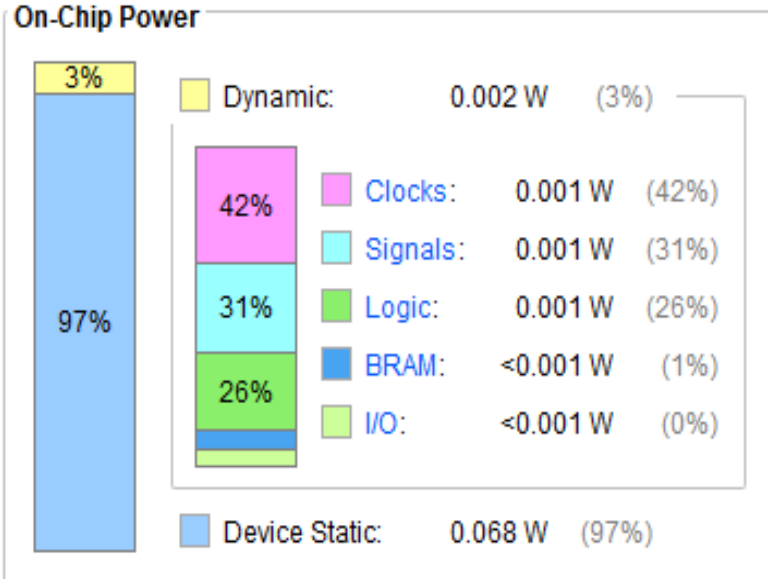
Now for a complex module, it is always recommendable to workout the issue with the help of creating the IP cores(ie…VIO, ILA);

- Complete the description in HDL(VHDL or Verilog) for a your logic.
- Verify its functional response through simulation.
- Create the cores with the total no. of modules sufficient to interface required set of inputs and outputs.
- Add the constraints (XDC) file (*get it from device vendor's website)
  - In general, it is from https://github.com/Digilent/digilent-xdc/, for Digitlent FPGA family
  - Bords- like., **ARTIX 7-XC7A35Tftg256-1**
- Carry out the Synthesis, Implementation and generate the bit file.
- Connect the corresponding h/w Board.
- Dump the bit file with the help of JTAG cable
- Verify the functional response with the VIO and ILA control signals through the Board

An illustration of Design process: ALU

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.071 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.3°C**
Thermal Margin:	59.7°C (12.2 W)
Effective ϑJA:	4.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



Setup

Worst Negative Slack (WNS):	26.931 ns
Total Negative Slack (TNS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	1041

Hold

Worst Hold Slack (WHS):	0.021 ns
Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	1033

Pulse Width

Worst Pulse Width Slack (WPWS):	15.250 ns
Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	487

All user specified timing constraints are met.

Useful Web links:

http://emicroelectronics.free.fr/onlineCourses/VLSI/toc.html
http://ece-research.unm.edu/jimp/vlsi/slides/c1_itrs.pdf
http://rti.etf.bg.ac.rs/rti/ri5rvl/tutorial/TUTORIAL/HTML/HOMEPG.HTM
https://www.tutorialspoint.com/vlsi_design/vlsi_design_useful_resources.htm
https://www.southampton.ac.uk/~bim/notes/cad/
http://www.uta.edu/ronc/4345sp02/lectures/
http://www.ece.utep.edu/courses/web5392/Lab_7.html
http://www.ece.utep.edu/courses/web5392/Notes.html
http://www.ittc.ku.edu/~jstiles/312/handouts/
https://www.mepits.com/tutorial/384/vlsi/steps-for-ic-manufacturing
https://personalpages.hs-kempten.de/~vollratj/Microelectronics/2017_04_24_06_Micro_DesignRules.html